

The AVR-D4-B generates a gate pulse and a DC drain bias for pulse testing of power MOSFETs, as per MIL-STD-750-3, Method 3472.2. The instrument mainframe connects to a test jig. The test jig accepts a variety of daughterboards. Each daughterboard will accept a specific package and pinout, and will have a specific resistance in series with the drain, and a specific resistance in series with the gate.

The gate pulse amplitude is adjustable from 5V to 10V, positive or negative. The pulse width is adjustable from 0.5 to 2 us, with < 10 ns rise times (at the input to  $R_{GATE}$ ).

The DC drain bias is adjustable from 20V to 225V, positive or negative. (The DC drain bias voltage will be the same polarity as the gate pulse.) The maximum drain pulse current is  $\pm 40$  A.

Attenuated replicas of the gate and drain voltage are provided on output connectors on the test jig. These waveforms must be measured with a user-supplied oscilloscope. The desired switching time values -  $t_{d(ON)}$ ,  $t_r$ ,  $t_{d(OFF)}$ ,  $t_f$  - may then be calculated from these waveforms.

The daughterboards are ordered separately, using the model number *AVX-D4-SLASH-PKG-RGATE-RDRAIN*. The parts in italics must be replaced as appropriate:

*-SLASH* code: Replace with the PRF-19500 slash sheet suffix (for example, -542J) that specifies the device package and pinout. (Devices without a matching slash sheet can be accommodated as well.)

*-PKG* code: Replace with the name of the package that will be accepted. Choose from -TO204AA, -TO204AE, -TO254AA, or -TO205AF. Other leaded packages can be readily accommodated. SMT package can also be handled, if the user specifies a readily-available socket or provides an appropriate socket.

*-RGATE* code: specify the gate resistance that will be installed on the daughterboard. Use "-7R5" for 7.5 $\Omega$ , for example. +/- 5% accuracy.

*-RDRAIN* code: specify the drain resistance that will be installed. Use "-28R1" for 28.1 $\Omega$ , for example. +/- 5% accuracy.

Avtech engineering staff can be easily contacted at [info@avtechpulse.com](mailto:info@avtechpulse.com) if you require assistance in configuring an appropriate system. These models can be customized readily to meet specific test requirements.

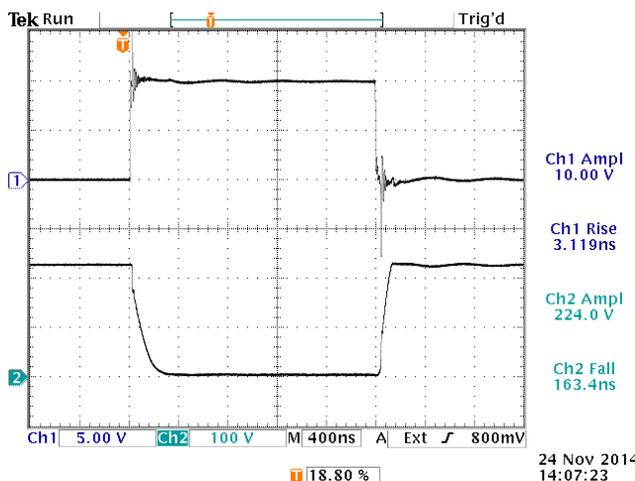
- Generates Method 3472.2 test waveforms
- Voltages to  $\pm 225$  Volts
- Amplitudes to  $\pm 40$  Amps
- Gate drive rise times less than 10 ns
- IEEE-488.2 GPIB and RS-232 interfaces
- Optional ethernet port for VXI-11.3 support

The AVR-D4-B includes a complete computer control interface. This provides GPIB and RS-232 computer-control, as well as front panel keypad and adjust knob control of the output pulse parameters. A large back-lit LCD displays the output amplitude, polarity, frequency, pulse width, and delay. To allow easy integration into automated test systems, the programming command set is based on the SCPI standard. For details, visit <http://www.avtechpulse.com/gpib>.

The -VXI option adds a rear-panel Ethernet connector, allowing the instrument to be remotely controlled using the VXI-11.3, ssh, telnet, and web protocols. In particular, the VXI-11.3 features allows software like LabView to control an instrument using standard VISA communications drivers and network cabling, instead of using older-style GPIB cabling and GPIB controller cards. For additional details, please see <http://www.avtechpulse.com/options/vxi>.

Avtech also offers a variety of pulse generators for use in recovery time tests (forward and reverse), bipolar junction transistor (BJT) switching time tests,  $dV/dt$  tests, and common mode transient immunity (CMTI) tests. For more information, please visit:

<http://www.avtechpulse.com/semiconductor>



Top: +10V gate drive, at input to  $R_{GATE} = 2.35\Omega$ .  
Bottom: +225V / +40A drain pulse ( $R_{DRAIN} = 5.6\Omega$ ).  
DUT: 2N6766 N-Channel MOSFET

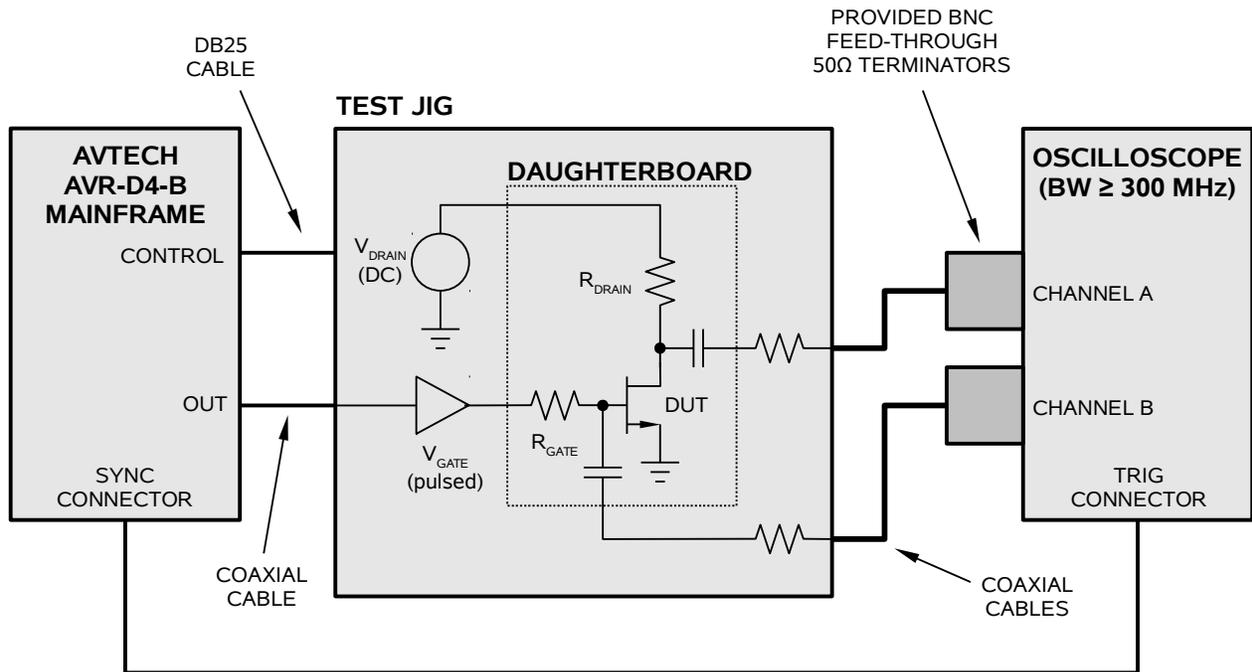
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|---|--|
| Model <sup>1</sup> :  | AVR-D4-B   |
| Basic test:   | The AVR-D4-B generates a gate pulse and a DC drain bias for pulse testing of power MOSFETs, as per MIL-STD-750-3, Method 3472.2. The instrument mainframe connects to a test jig. The test jig accepts a variety of daughterboards. Each daughterboard will accept a specific package and pinout, and will have a specific resistance in series with the drain, and a specific resistance in series with the gate.   |
| Gate pulse amplitude:   | 5V to 10V, positive or negative.   |
| Gate pulse width (FWHM):  | 0.5 us to 2 us   |
| Gate rise time (20%-80%):   | < 10 ns, at input to R <sub>GATE</sub>   |
| Minimum allowed R <sub>GATE</sub> :                                   | 2.2 Ω  |
| Pulse repetition frequency:   | 1 to 100 Hz  |
| DC drain bias:  | 20V to 225V. Same polarity as gate pulse.  |
| Maximum drain pulse current:  | ± 40 A   |
| Included daughterboards:  | <p>None. The daughterboards are ordered separately, using the model number <i>AVX-D4-SLASH-PKG-RGATE-RDRAIN</i>. The parts in italics must be replaced with:</p> <ul style="list-style-type: none"> <li>-SLASH code: Replace with the PRF-19500 slash sheet suffix (for example, -542J) that specifies the device package and pinout.</li> <li>-PKG code: Replace the "-PKG" suffix with the name of the package that will be accepted. Choose from -TO204AA, -TO204AE, -TO254AA, or -TO205AF. Other leaded packages can be readily accommodated. SMT packages can also be handled, if the user specifies a readily-available socket or provides an appropriate socket.</li> <li>-RGATE code: specify the gate resistance that will be installed on the daughterboard. Use "-7R5" for 7.5Ω, for example. +/- 5% accuracy.</li> <li>-RDRAIN code: specify the drain resistance that will be installed on the daughterboard. Use "-28R1" for 28.1Ω, for example. +/- 5% accuracy.</li> </ul> |
| Outputs:  | Two voltage waveforms (gate and drain) must be monitored on a user-provided oscilloscope to measure t <sub>d(on)</sub> , t <sub>d(off)</sub> , t <sub>r</sub> , and t <sub>f</sub> . The AVR-D4-B itself does not include any measurement functionality.   |
| Propagation delay:  | ≤ 150 ns (Ext trig in to pulse out)  |
| Jitter:   | ± 100 ps ± 0.03% of sync delay (Ext trig in to pulse out)  |
| Trigger modes:  | Internal trigger, external trigger (TTL level pulse, > 10 ns, 1 kΩ input impedance), front-panel "Single Pulse" pushbutton, or single pulse trigger via computer command.  |
| Variable delay:   | Sync to main out: 0 to 1.0 seconds, for all trigger modes (including external trigger).  |
| Sync output:  | > +3 Volts, > 50 ns, will drive 50 Ohm loads   |
| Gated operation:  | Active high or low, switchable.  |
| Connectors:   | Out, Trig, Sync, Gate: BNC   |
| GPIB & RS-232 control <sup>1</sup> :                                  | Standard feature on all -B units.  |
| Ethernet port, for remote control using VXI-11.3, ssh, telnet, & web: | Optional <sup>2</sup> . Recommended as a modern alternative to GPIB / RS-232. See <a href="http://www.avtechpulse.com/options/vxi">http://www.avtechpulse.com/options/vxi</a> for details.   |
| Settings resolution:  | The resolution of the timing parameters (pulse width, delay, period) varies, but is always better than 0.15% of ( set value  + 20 ns). The amplitude resolution is < 0.1% of the maximum amplitude.  |
| Settings accuracy:  | Typically ± 3% (plus ±1V or ± 2 ns) after 10 minute warmup. For high-accuracy applications requiring traceable calibration, verify the output parameters with a calibrated oscilloscope.   |
| Power requirements:   | 100 - 240 Volts, 50 - 60 Hz  |
| Dimensions:   | 100 mm x 430 mm x 375 mm (3.9" x 17" x 14.8")  |
| Chassis material:   | Cast aluminum frame and handles, blue vinyl on aluminum cover plates   |
| Mounting:   | Any. Add -R5 to the model number to add a rack-mount kit.  |
| Temperature range:  | +5°C to +40°C  |

1)-B suffix indicates IEEE-488.2 GPIB and RS-232 control of amplitude and frequency. See <http://www.avtechpulse.com/gpib> for details.

2)Add the suffix -VXI to the model number to specify the Ethernet port.



## TYPICAL TEST ARRANGEMENT



## STANDARD TEST JIG, WITH A TYPICAL DAUGHTERBOARD INSTALLED

