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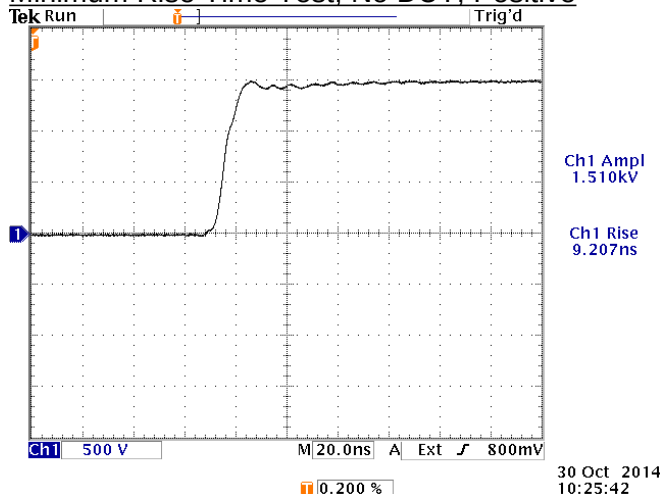
BOX 5120, LCD MERIVALE
OTTAWA, ONTARIO
CANADA K2C 3H5

info@avtechpulse.com - http://www.avtechpulse.com/

PERFORMANCE CHECKSHEET

Model: AVRQ-5-B
Type: Common Mode Transient Immunity (CMTI) Test for Opto-Couplers
S.N.: 00001 (internal model)
Date: October 30, 2014

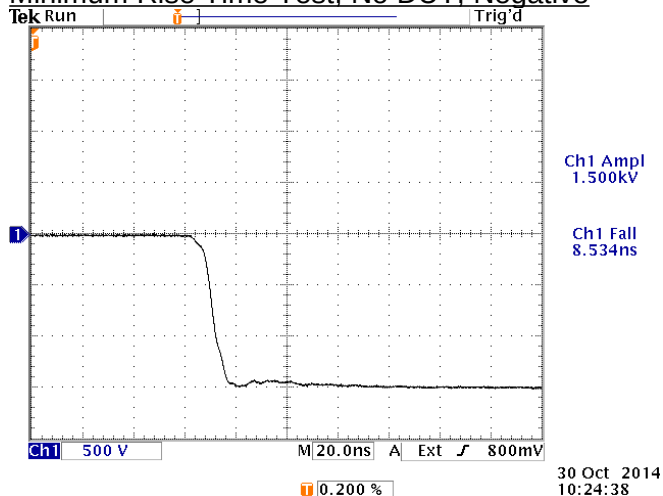
Minimum Rise Time Test, No DUT, Positive



- a) Output Signal Amplitude: ± 1.5 kV
- b) Rise Time (10%-90%): 10 – 50 ns
- c) PRF: 1 Hz - 10 Hz
- d) Jitter, Stability: OK
- e) Prime Power: 100-240V AC, 50-60 Hz.

A daughterboard is installed in the ZIF socket, but no DUT or capacitance is installed on the daughterboard.

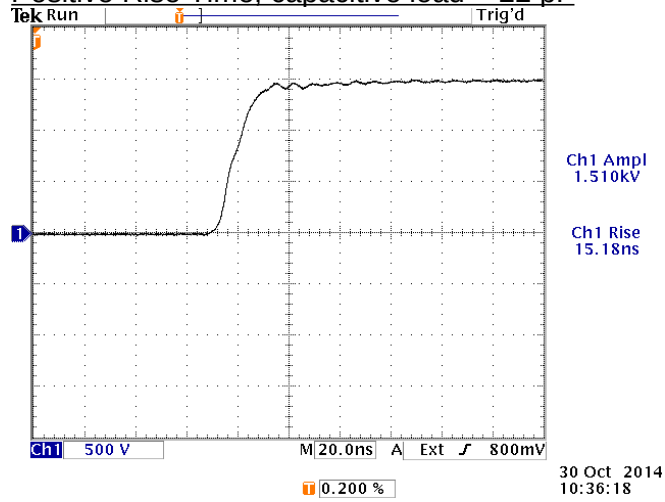
Minimum Rise Time Test, No DUT, Negative



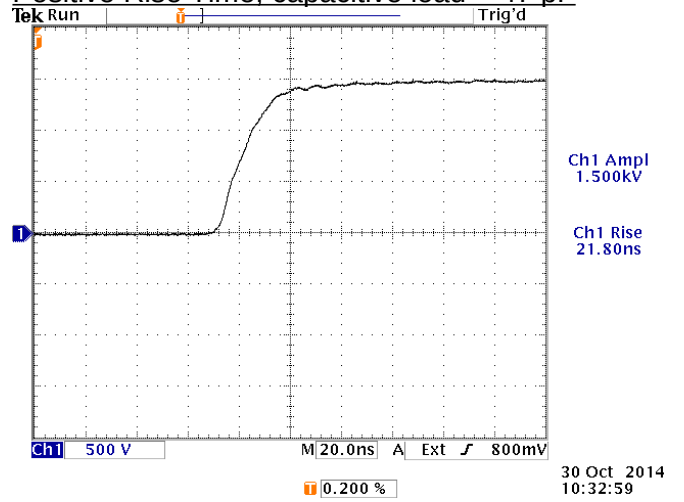
A daughterboard is installed in the ZIF socket, but no DUT or capacitance is installed on the daughterboard.

Daughterboard installed in ZIF socket, in positive position

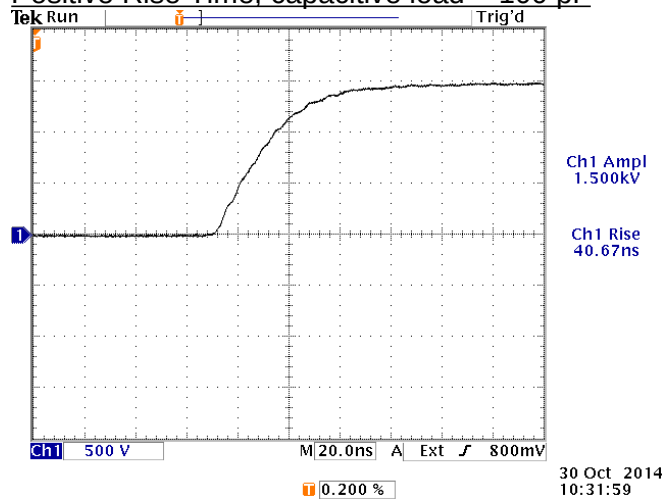
Positive Rise Time, capacitive load = 22 pF



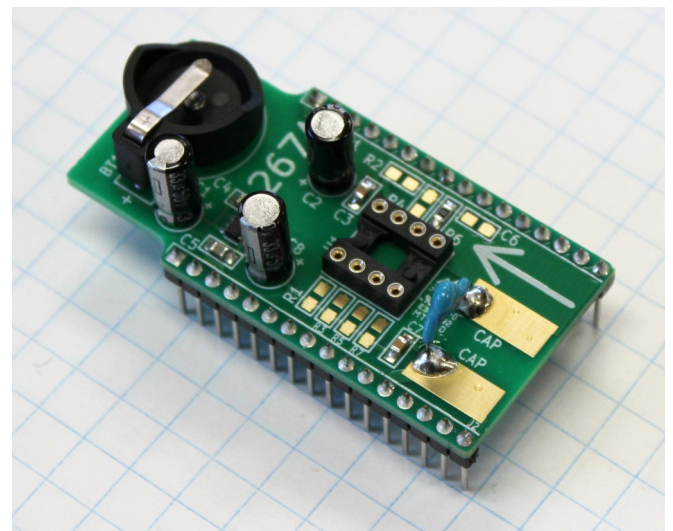
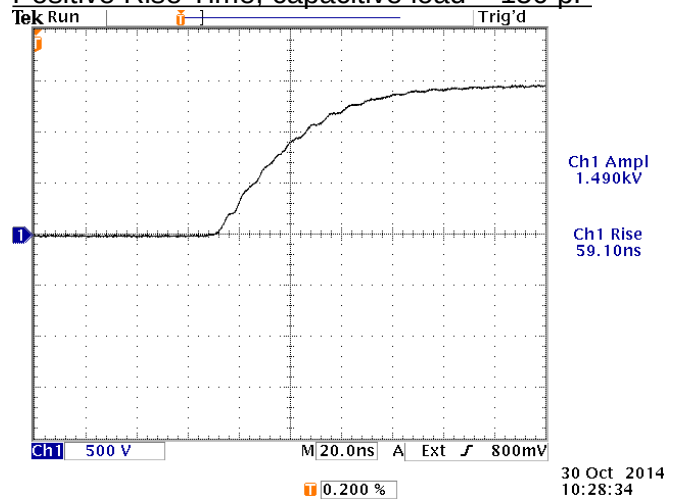
Positive Rise Time, capacitive load = 47 pF



Positive Rise Time, capacitive load = 100 pF

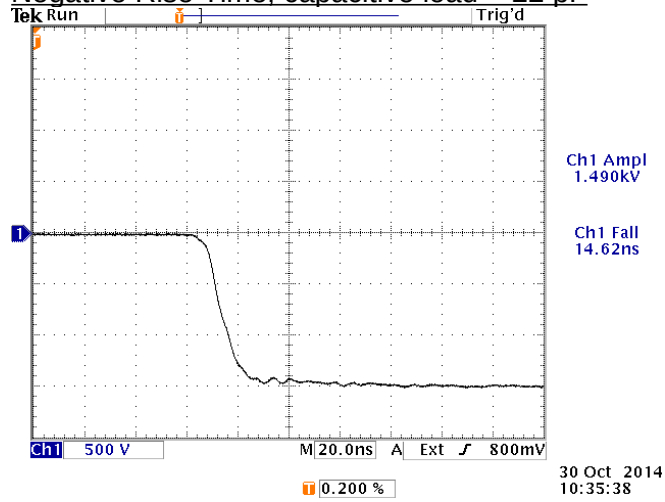


Positive Rise Time, capacitive load = 150 pF

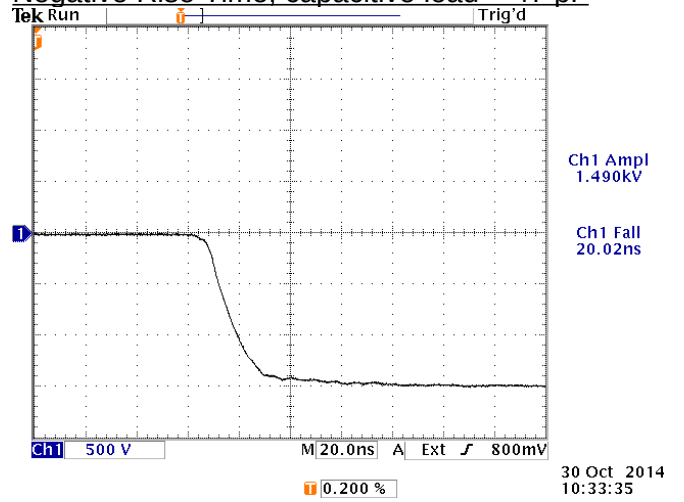


22 pF capacitor (blue) on daughterboard

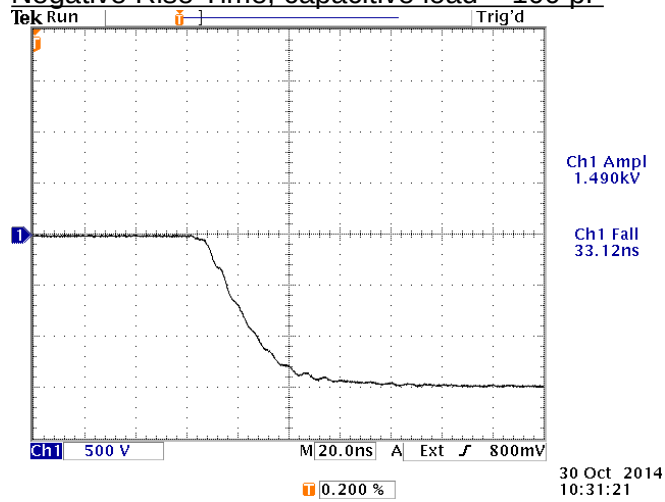
Negative Rise Time, capacitive load = 22 pF



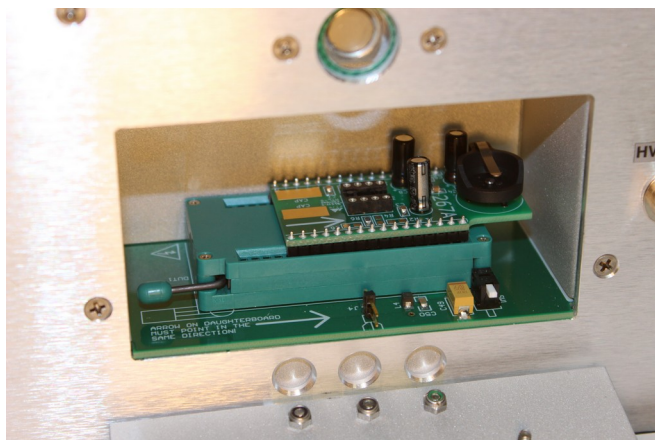
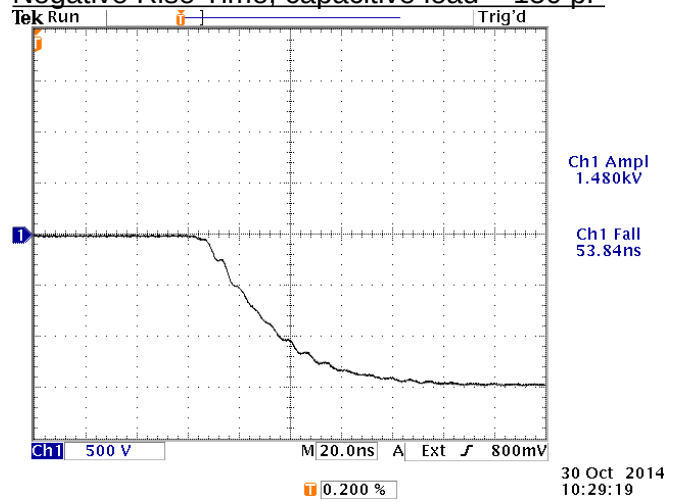
Negative Rise Time, capacitive load = 47 pF



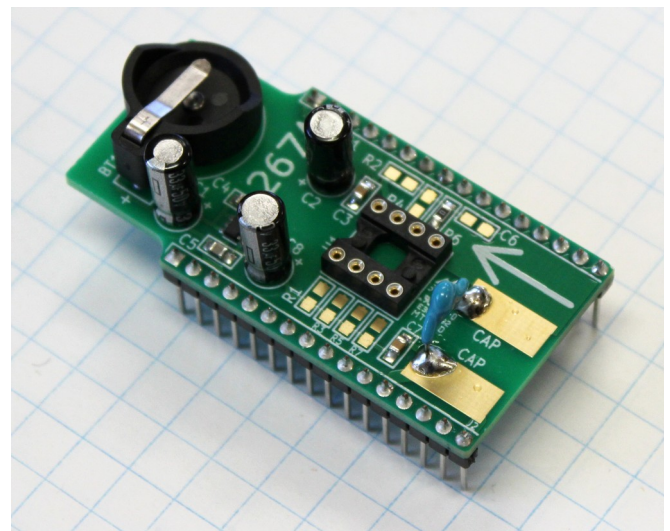
Negative Rise Time, capacitive load = 100 pF



Negative Rise Time, capacitive load = 150 pF

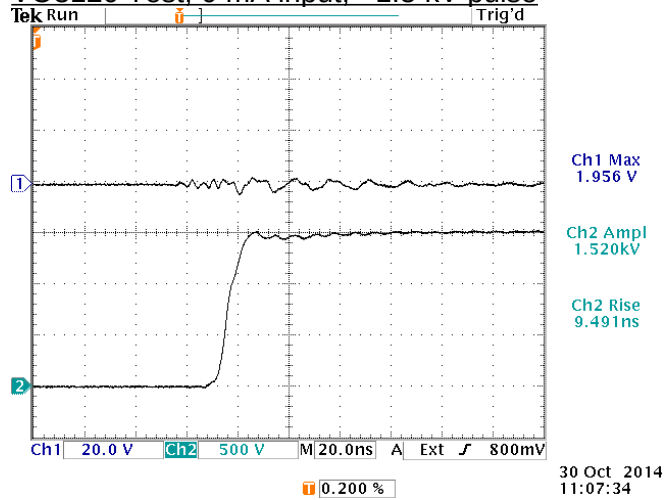


Daughterboard installed in ZIF socket, in negative position



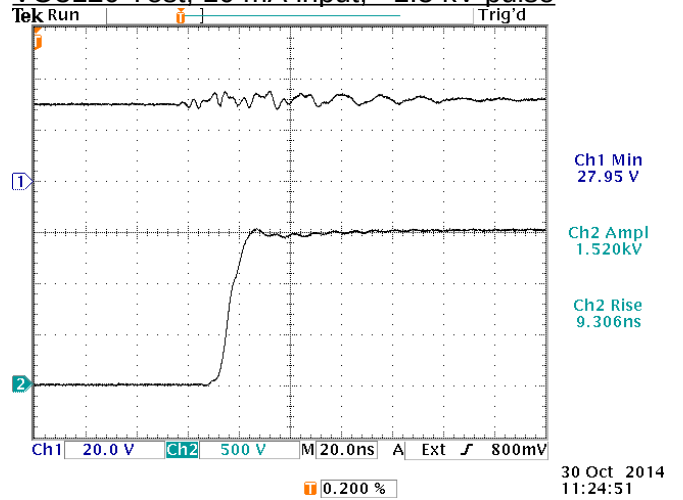
22 pF capacitor (blue) on daughterboard

VO3120 Test, 0 mA input, +1.5 kV pulse



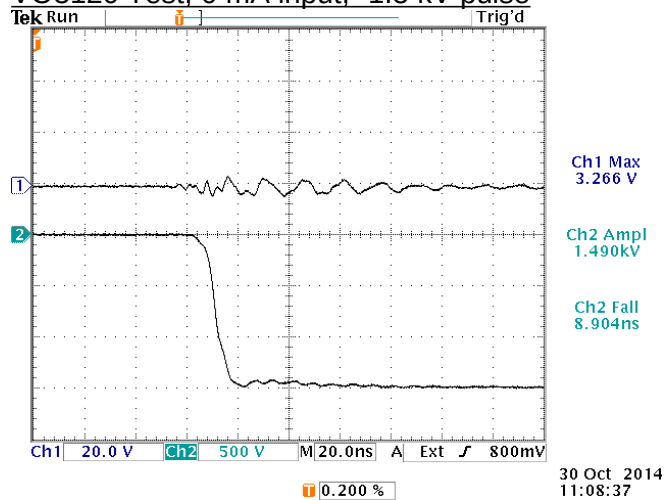
Top = Logic output (with +32V supply). No glitch.
Bottom = high voltage pulse

VO3120 Test, 10 mA input, +1.5 kV pulse



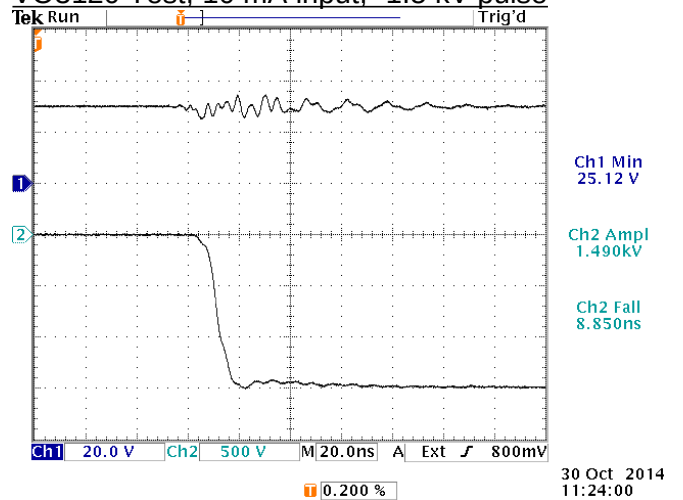
Top = Logic output (with +32V supply). No glitch.
Bottom = high voltage pulse

VO3120 Test, 0 mA input, -1.5 kV pulse

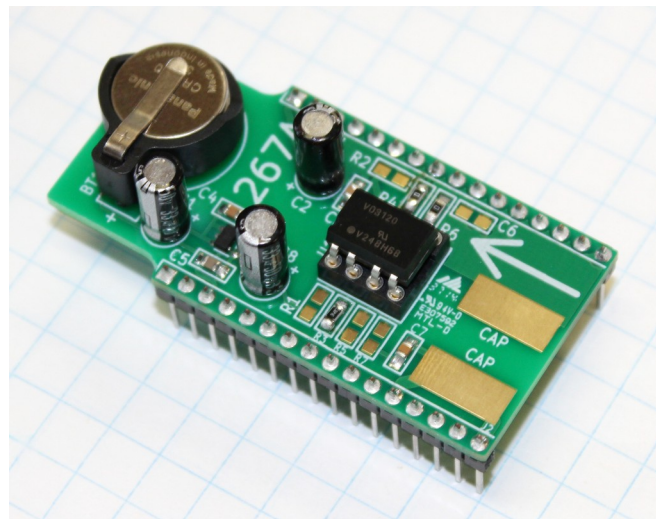


Top = Logic output (with +32V supply). No glitch.
Bottom = high voltage pulse

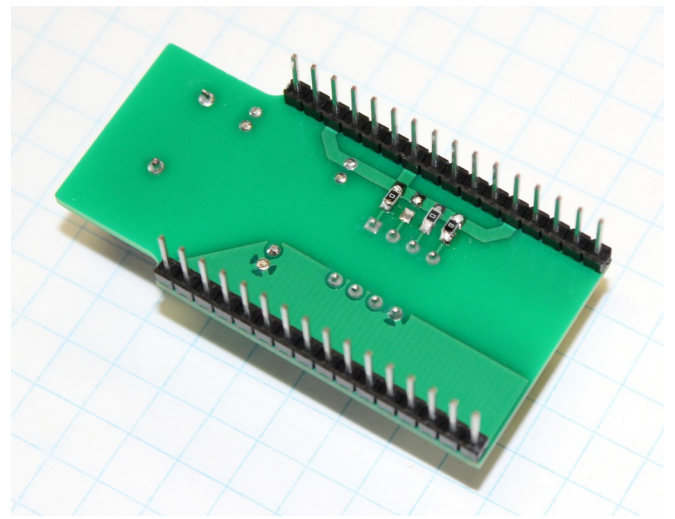
VO3120 Test, 10 mA input, -1.5 kV pulse



Top = Logic output (with +32V supply). No glitch.
Bottom = high voltage pulse

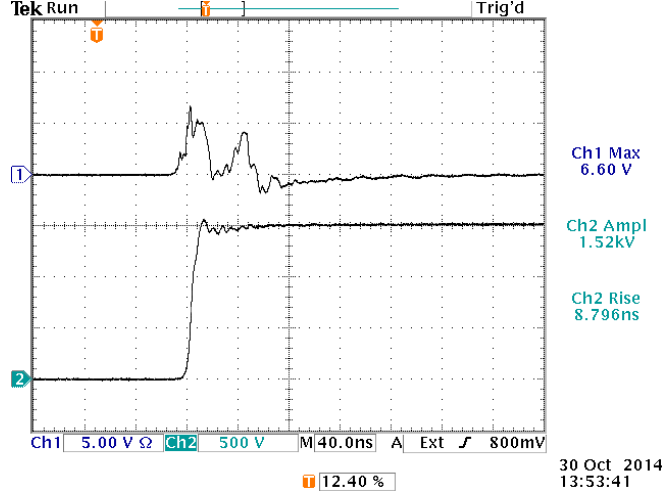


Top side of daughterboard with VO3120 configured for 10 mA bias.



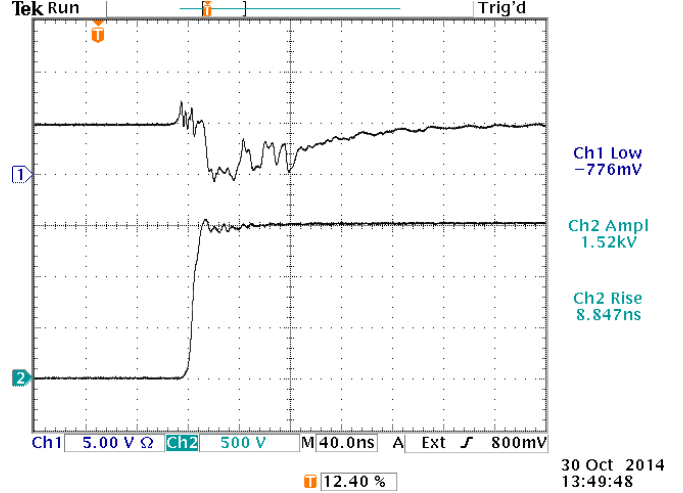
Bottom side of daughterboard with VO3120 configured for 10 mA bias.

HCPL-7721 Test, 0V input, +1.5 kV pulse



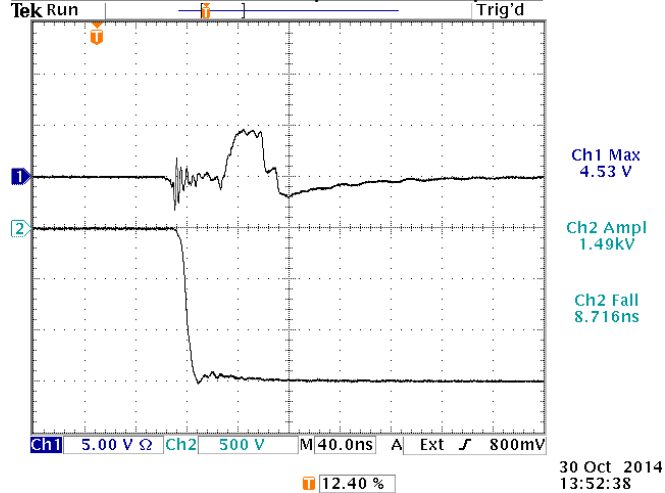
Top = Logic output (with +5V supply). Glitch.
Bottom = high voltage pulse

HCPL-7721 Test, 5V input, +1.5 kV pulse



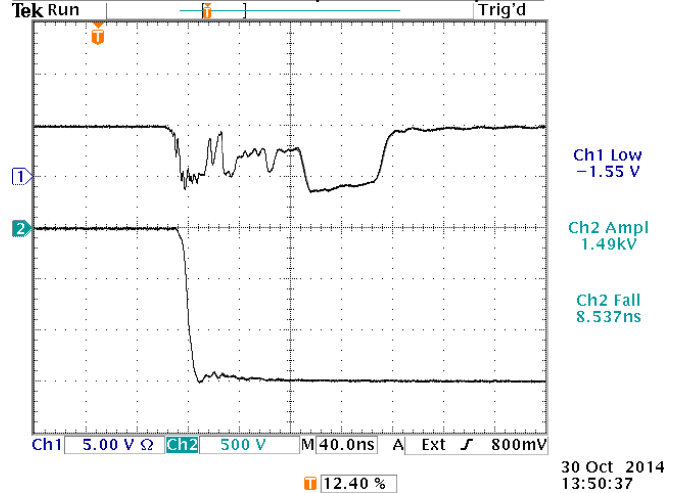
Top = Logic output (with +5V supply). Glitch.
Bottom = high voltage pulse

HCPL-7721 Test, 0V input, -1.5 kV pulse

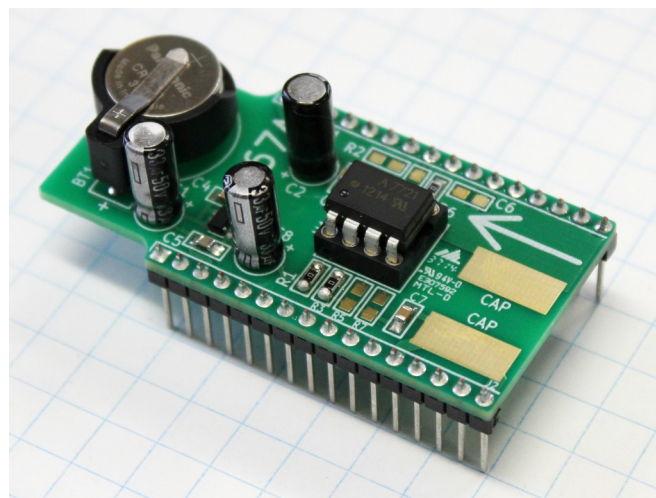


Top = Logic output (with +5V supply). Glitch.
Bottom = high voltage pulse

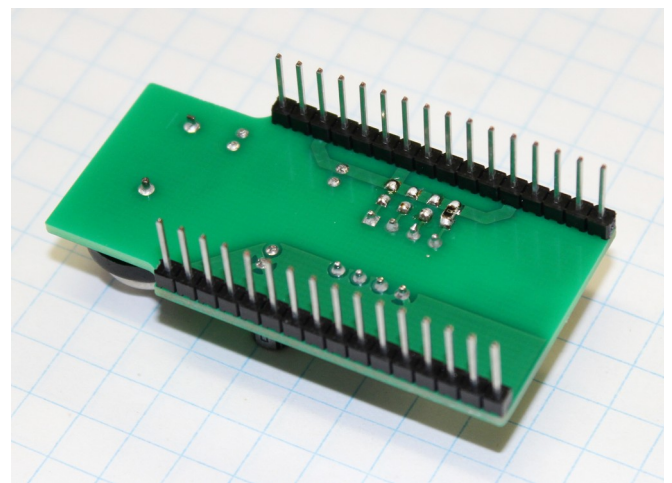
HCPL-7721 Test, 5V input, -1.5 kV pulse



Top = Logic output (with +5V supply). Glitch.
Bottom = high voltage pulse

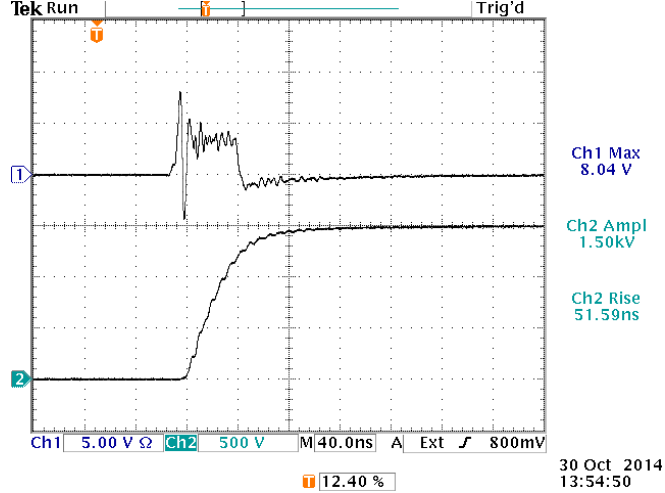


Top side of daughterboard with HCPL-7721 configured for 5V bias.



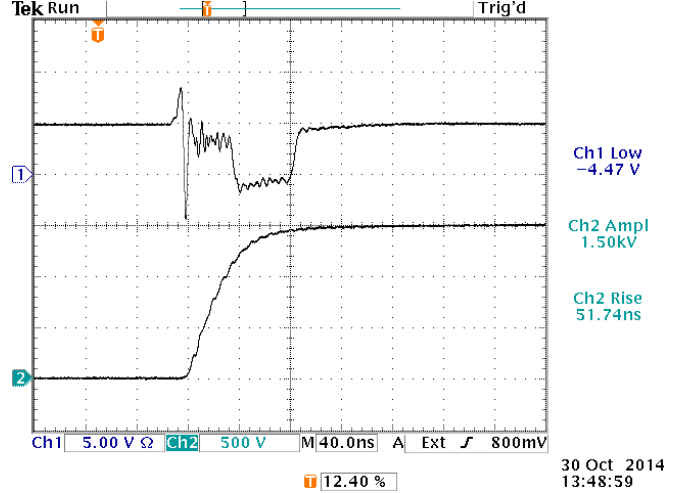
Bottom side of daughterboard with HCPL-7721 configured for 5V bias.

HCPL-7721, 0V input, +1.5 kV, 150 pF added



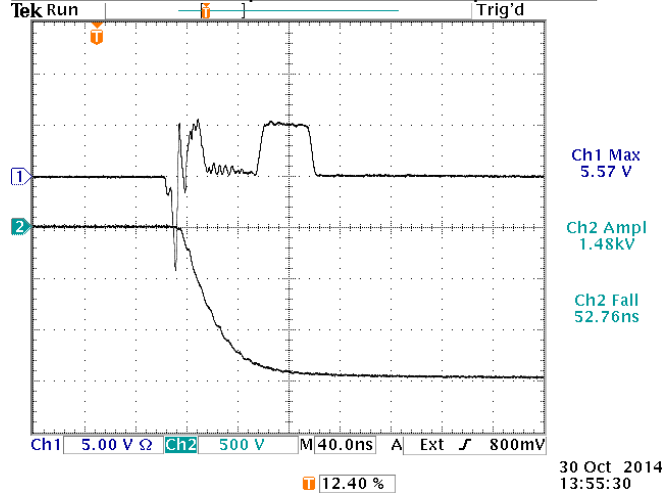
Top = Logic output (with +5V supply). Glitch.
Bottom = high voltage pulse

HCPL-7721, 5V input, +1.5 kV, 150 pF added



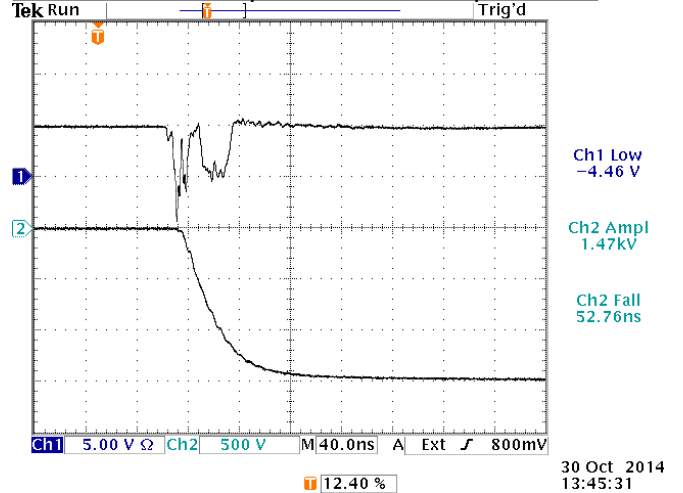
Top = Logic output (with +5V supply). Glitch.
Bottom = high voltage pulse

HCPL-7721, 0V input, -1.5 kV, 150 pF added



Top = Logic output (with +5V supply). Glitch.
Bottom = high voltage pulse

HCPL-7721, 5V input, -1.5 kV, 150 pF added



Top = Logic output (with +5V supply). Glitch.
Bottom = high voltage pulse