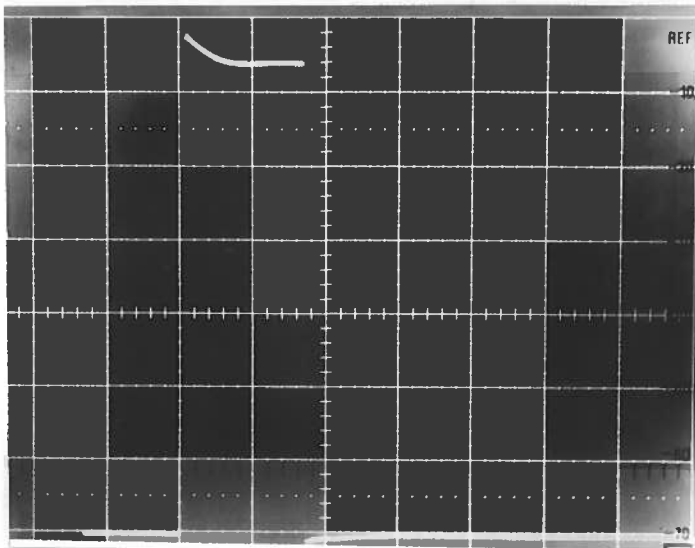


PULSE GENERATOR  
PERFORMANCE CHECK

Model: *AVR-7B-C-PN-AT*

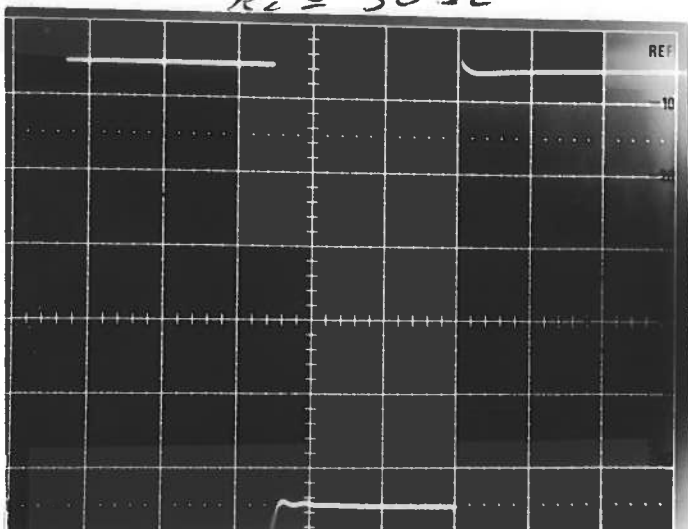
S.N.: *5855*

Date: *APRIL 12 1991*



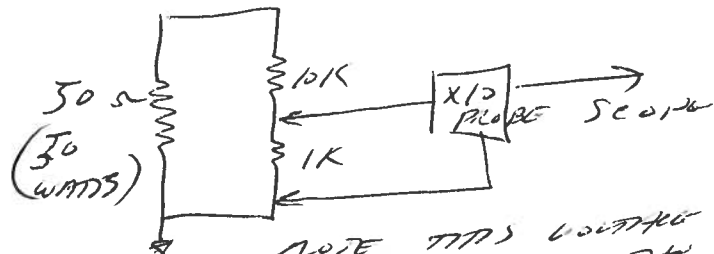
- a) Output signal amplitude:  
*0 TO ± 700 VOLTS*
- b) Pulse width:  
*0.1 TO 100 μS*
- c) Rise time:  
*0.5% MAX DUTY CYCLE*  
*≤ 50 μS*
- d) Fall time:  
*≤ 50 NS*
- e) PRF: *6 TO 10 KHz*  
*0.5% MAX DUTY*
- f) Jitter, stability: *CYCLES*
- g) Prime power: *6K*  
*120/240 V*  
*50-60 Hz*

*P<sub>out</sub> 1 μS/div*  
*≈ 100 VOLTS/div*  
*R<sub>L</sub> = 50 Ω*



*N<sub>out</sub> 10 μS/div*  
*≈ 100 VOLTS/div*  
*R<sub>L</sub> = 50 Ω*

RESISTIVE LOAD



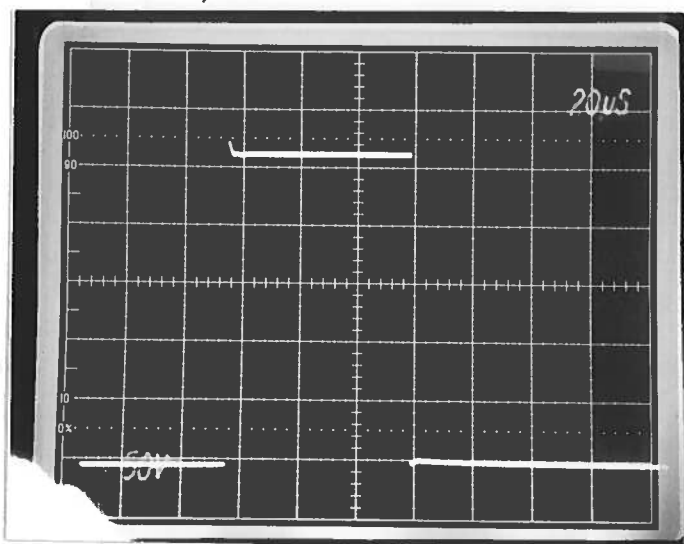
*NOTE THIS VOLTAGE DIVIDER CIRCUIT THE APPROPRIATE OVERLOAD ON THE WAVEFORM*

PULSE GENERATOR  
PERFORMANCE CHECK

Model: APR-7B-C-PW-AT

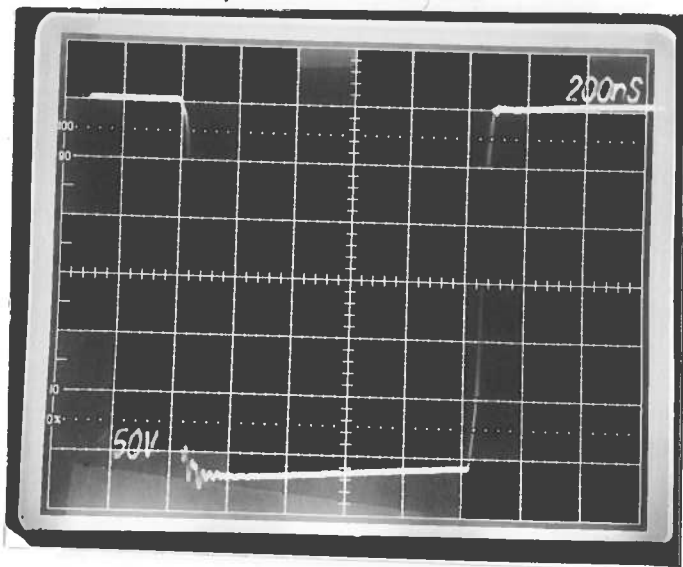
S.N.: 5855

Date: DEC 22 1994



- a) Output signal amplitude:  
 $0 \text{ TO } \pm 700 \text{ VOLTS TO}$
- b) Pulse width:  $R_L \geq 50 \Omega$   
 $0.1 \text{ TO } 100 \mu\text{S}$
- c) Rise time:  $(0.5\% \text{ MAX DUTY CYCLE})$   
 $\leq 50 \text{ NS}$
- d) Fall time:  
 $\leq 50 \text{ NS}$
- e) PRF:  $0 \text{ TO } 10 \text{ KHz}$   
 $(0.5\% \text{ MAX DUTY CYCLE})$
- f) Jitter, stability:  $(0.5\% \text{ MAX DUTY CYCLE})$
- g) Prime power:  $OK$   
 $120/240 \text{ V}$   
 $50-60 \text{ Hz}$

Ⓐ POINT:  $R_L = 50 \Omega$   
50 V/DIV



Ⓑ POINT:  $R_L = 50 \Omega$   
50 V/DIV  
PRF = 1 KHz