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SINCE 1975

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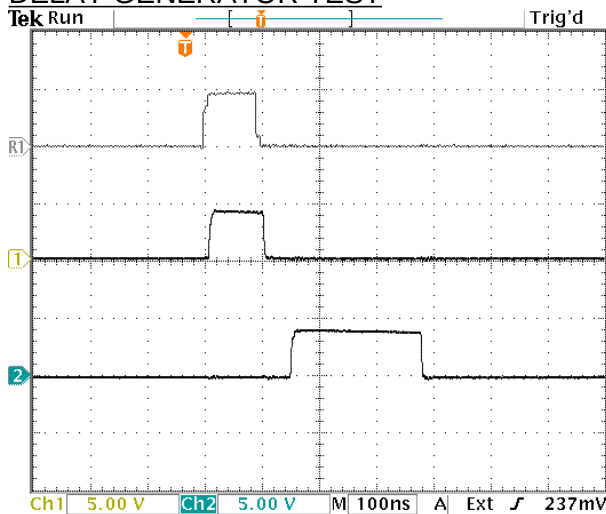
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PERFORMANCE CHECKSHEET

Model: AVX-D-PS-ED-SMA
S.N.: 10766
Date: November 4, 2003

DELAY GENERATOR TEST



4 Nov 2003
14:16:32

Top: Input signal – TTL pulse.

Middle: TRIG output.

Bottom: OUT output. Delay set at maximum (150 ns)

Input-to-output jitter, at maximum delay, as measured by Fluke PM6681: 33 ps (std. dev.). (The noise floor of the Fluke PM6681 is approximately 25-30 ps.)

a) Output Signal Amplitude: TTL, to 50Ω

b) Pulse Width - TRIG: $PW_{OUT} = PW_{IN}$
- OUT: 250 ns, approx

c) Delay: 30 ns to 150 ns

d) PRF: 1 MHz maximum

e) Jitter, Stability: OK

f) Prime Power: 100-240V, 50-60 Hz.

COMPOSITE SYSTEM TEST

A 1 kHz, 300 mV, 20 ns wide signal was applied to the AVX-STRB-PS (S/N 10765) input. The AVX-STRB-PS output triggered the AVX-D-PS-ED-SMA (S/N 10766), whose delay was set to maximum. The AVX-D-PS-ED-SMA output triggered the AVR-E4-C-P-SMA-ED (S/N 10764), which was set at maximum pulse width and amplitude. The jitter measured between the 300 mV input and the 100V output was 33 ps (std. dev.).