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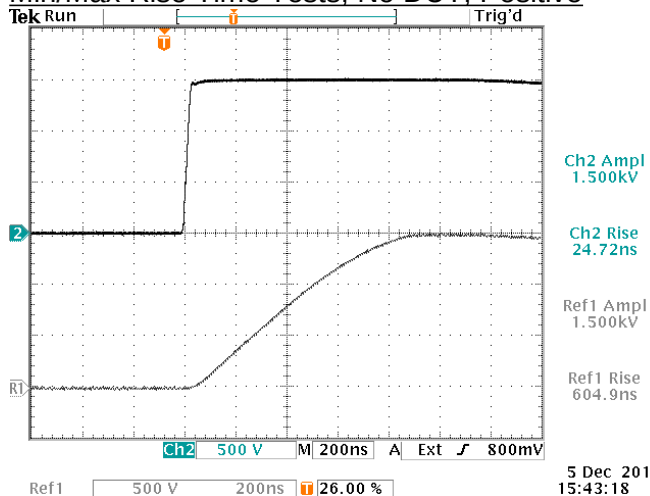
BOX 5120, LCD MERIVALE  
OTTAWA, ONTARIO  
CANADA K2C 3H5

info@avtechpulse.com - http://www.avtechpulse.com/

PERFORMANCE CHECKSHEET

Model: AVRQ-4-B-ATA3-SCHB  
Type: Common Mode Transient Immunity (CMTI) Test for Opto-Couplers  
S.N.: 13104  
Date: December 5, 2013

Min/Max Rise Time Tests, No DUT, Positive



a) Output Signal Amplitude: ±1 kV, ±1.5 kV

b) Rise Time (10%-90%): 25 ns - 250 ns

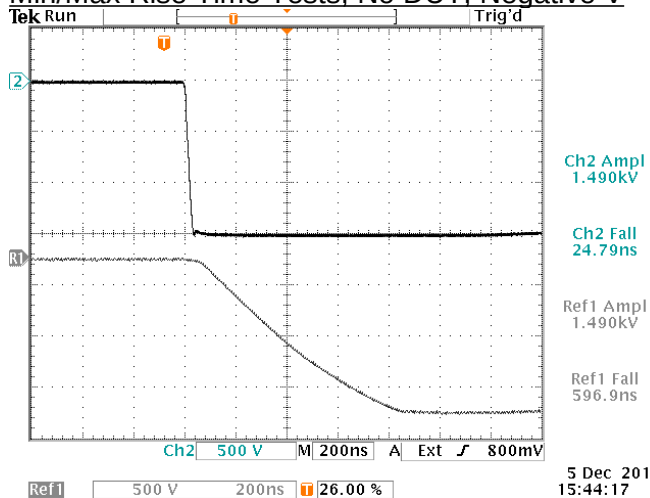
c) PRF: 1 Hz - 10 Hz

d) Jitter, Stability: OK

e) Prime Power: 100-240V AC, 50-60 Hz.

Top: minimum rise time setting, +1.5 kV  
Bottom: maximum rise time setting, +1.5 kV

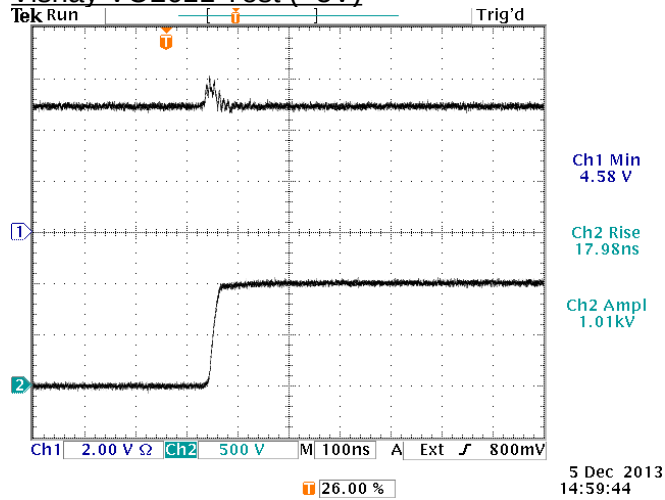
Min/Max Rise Time Tests, No DUT, Negative V



Top: minimum rise time setting, -1.5 kV  
Bottom: maximum rise time setting, -1.5 kV

References levels: 10%, 90%.

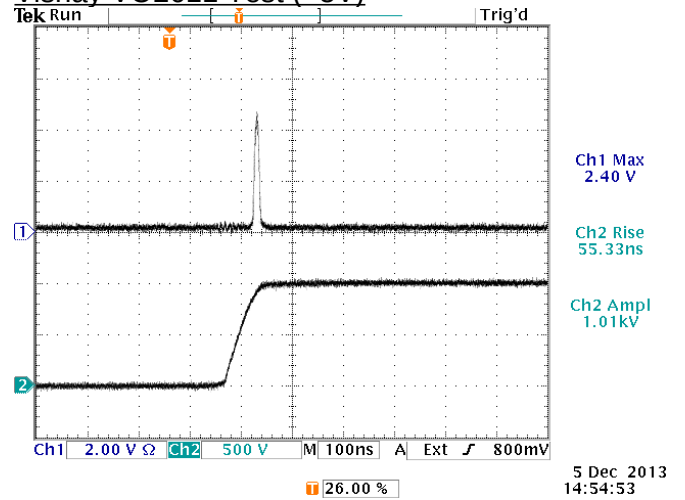
### Vishay VO2611 Test (+5V)



+1kV, +5V, 0 mA, 348Ω load ("A" PCB).

No glitches at minimum risetime, so the CMTI exceeds  $(1\text{kV} \times (90\% - 10\%)) / 17.98\text{ ns} = 44.5\text{ kV/us}$ .

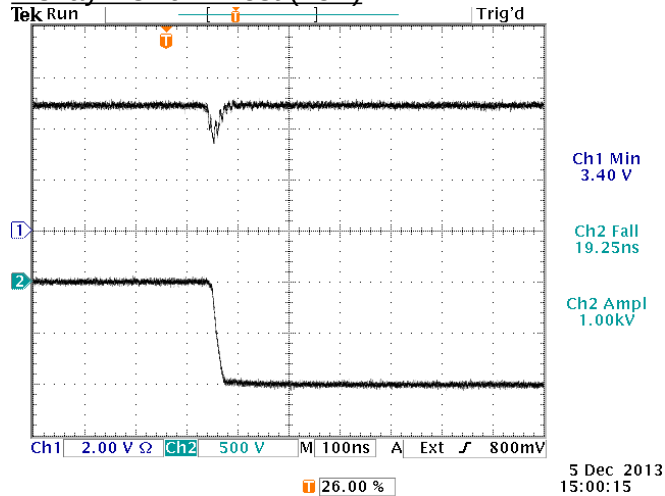
### Vishay VO2611 Test (+5V)



+1kV, +5V, 7.5 mA, 348Ω load ("D" PCB).

A glitch starts to occur at  $1\text{ kV} \times (90\% - 10\%) / 55.33\text{ ns} = 14.5\text{ kV/us}$ , which is less than the 15 kV/us specification.

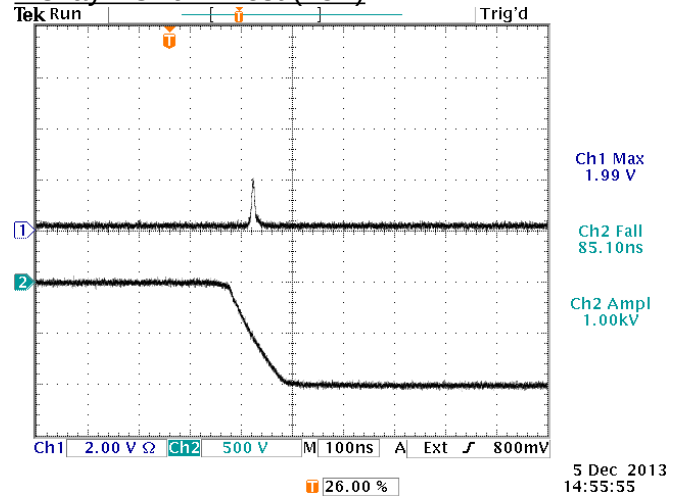
### Vishay VO2611 Test (+5V)



-1kV, +5V, 0 mA, 348Ω load ("A" PCB).

No glitches at minimum risetime, so the CMTI exceeds  $(1\text{kV} \times (90\% - 10\%)) / 19.25\text{ ns} = 41.6\text{ kV/us}$ .

### Vishay VO2611 Test (+5V)

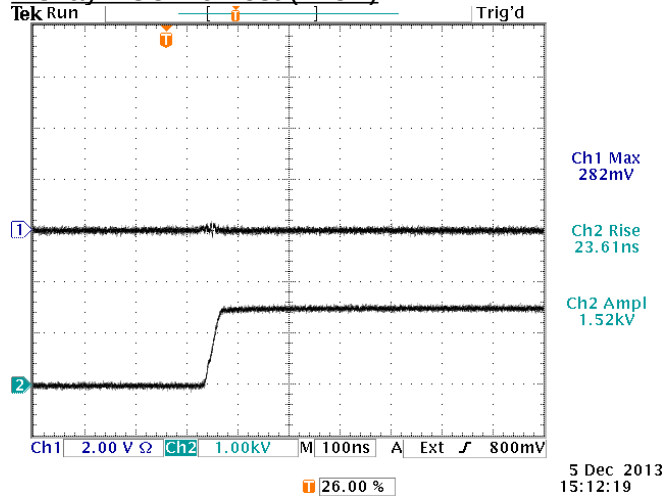


-1kV, +5V, 7.5 mA, 348Ω load ("D" PCB).

A glitch starts to occur at  $1\text{ kV} \times (90\% - 10\%) / 85.10\text{ ns} = 9.4\text{ kV/us}$ , which is less than the 15 kV/us specification.

The two DUTs used in the tests on this page remain installed on the "A" and "D" daughterboards, for customer comparison and testing purposes. Both have the "V 051H68" datecode.

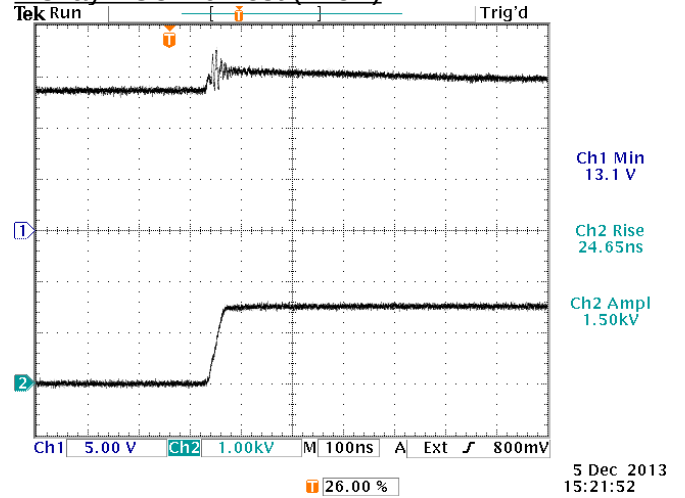
### Vishay VO3120 Test (+15V)



+1.5kV, +15V, 0 mA

No glitches at minimum risetime, so the CMTI exceeds  $(1.5\text{kV} \times (90\% - 10\%) / 23.61\text{ ns}) = 50.8\text{ kV/us}$ .

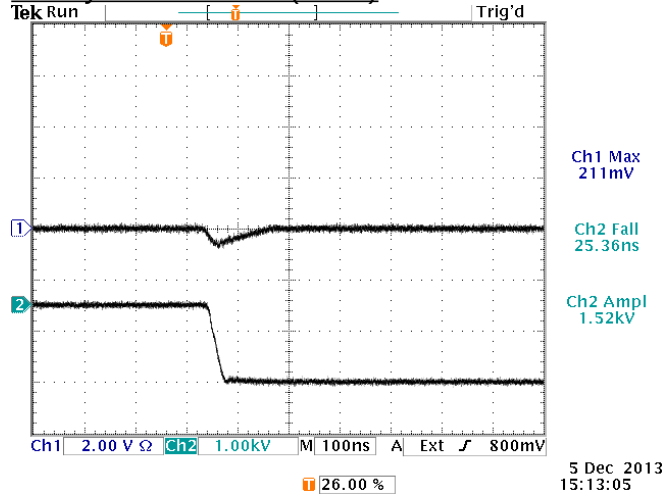
### Vishay VO3120 Test (+15V)



+1.5kV, +15V, 10 mA

No glitches at minimum risetime, so the CMTI exceeds  $(1.5\text{kV} \times (90\% - 10\%) / 24.65\text{ ns}) = 48.7\text{ kV/us}$ .

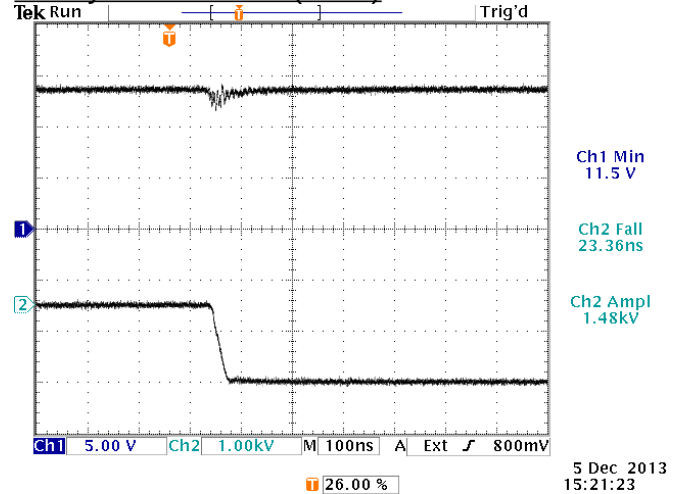
### Vishay VO3120 Test (+15V)



-1.5kV, +15V, 0 mA

No glitches at minimum risetime, so the CMTI exceeds  $(1.5\text{kV} \times (90\% - 10\%) / 25.36\text{ ns}) = 47.3\text{ kV/us}$ .

### Vishay VO3120 Test (+15V)



-1.5kV, +15V, 10 mA

No glitches at minimum risetime, so the CMTI exceeds  $(1.5\text{kV} \times (90\% - 10\%) / 23.36\text{ ns}) = 51.4\text{ kV/us}$ .

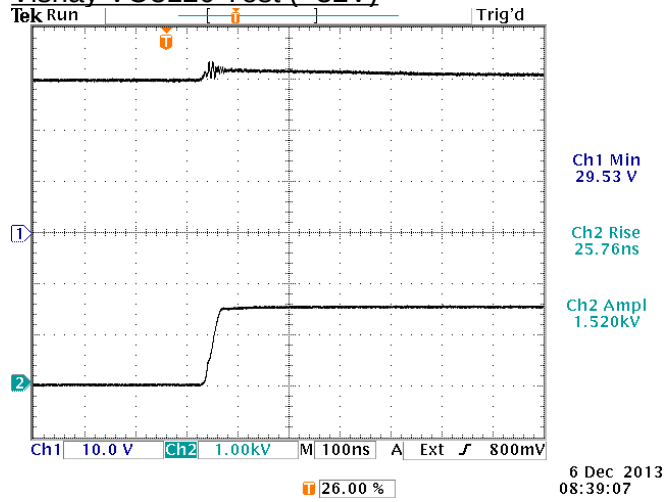
A P6139A probe was used to measure the logic output, instead of the P6246 differential probe, due to its limited voltage input range.

A non-standard daughterboard was used to test the VO3120, with:

- R1, R2, R5, R7, C6: unused
- R4, R6, R8, R10, R11: zero Ohms
- R3 = unused for 0 mA, 348 Ohms for 10 mA
- R9 = zero Ohms for 0 mA, unused for 10 mA

This daughterboard and DUT were retained at the factory, and not shipped.

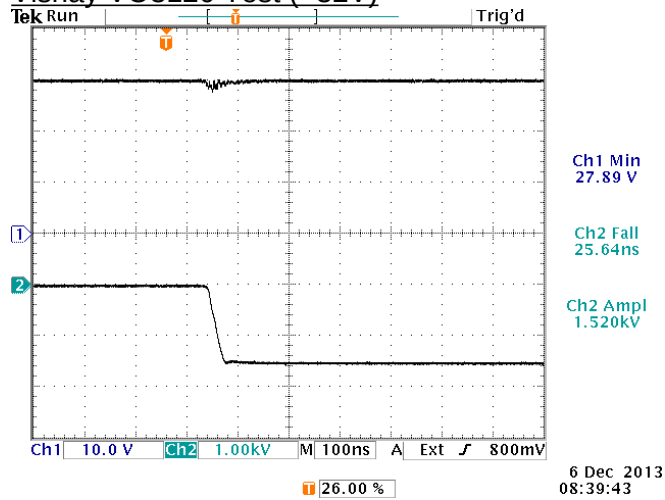
### Vishay VO3120 Test (+32V)



+1.5kV, +32V, 10 mA

No glitches at minimum risetime, so the CMTI exceeds  $(1.5\text{kV} \times (90\% - 10\%) / 25.76 \text{ ns}) = 46.6 \text{ kV/us}$ .

### Vishay VO3120 Test (+32V)



-1.5kV, +32V, 10 mA

No glitches at minimum risetime, so the CMTI exceeds  $(1.5\text{kV} \times (90\% - 10\%) / 25.64 \text{ ns}) = 46.8 \text{ kV/us}$ .