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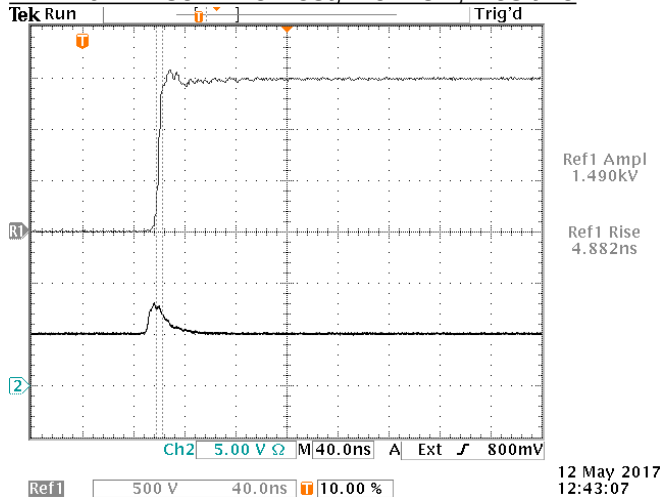
BOX 5120, LCD MERIVALE  
OTTAWA, ONTARIO  
CANADA K2C 3H5

info@avtechpulse.com - http://www.avtechpulse.com/

PERFORMANCE CHECKSHEET

Model: AVRQ-5-B-FPD-ATA3-AC03  
Type: Common Mode Transient Immunity (CMTI) Test for Opto-Couplers  
S.N.: 13432 (repaired / modified)  
Date: May 12, 2017

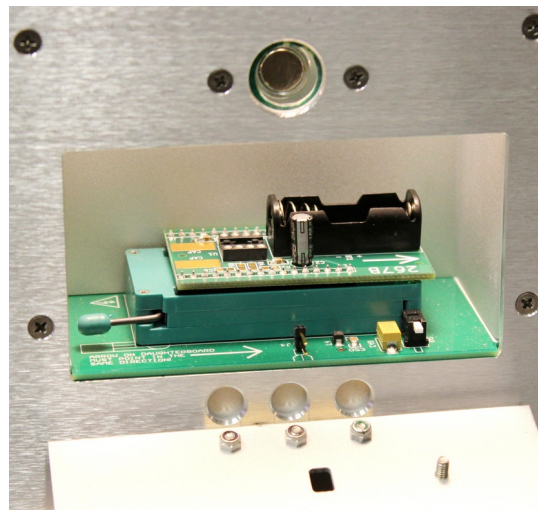
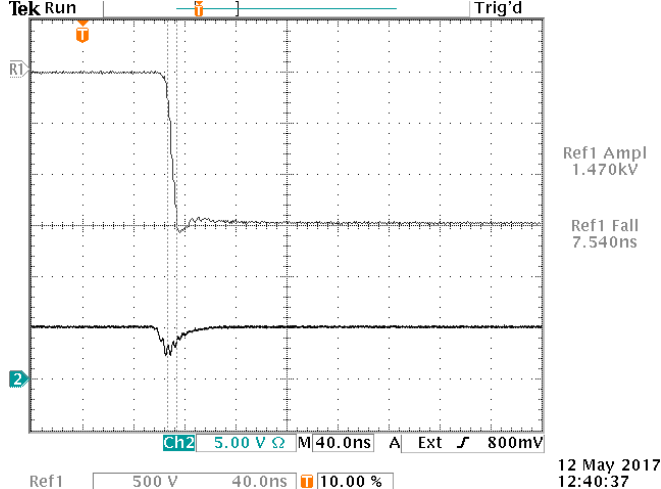
Minimum Rise Time Test, No DUT, Positive



- a) Output Signal Amplitude:  $\pm 1.5$  kV
- b) Rise Time (10%-90%): < 10 to > 50 ns
- c) PRF: 1 Hz - 10 Hz
- d) Jitter, Stability: OK
- e) Prime Power: 100-240V AC, 50-60 Hz.

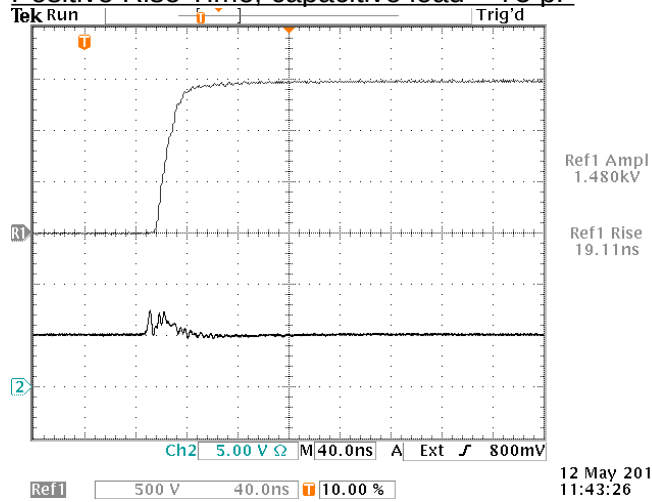
Top = HV out. Bottom = Logic out, VCC2 = +5V, using P6246, and no DUT, R2 = 1 k $\Omega$ . (This shows the parasitic capacitive coupling onto the logic output. See the manual for details.)

Minimum Rise Time Test, No DUT, Negative

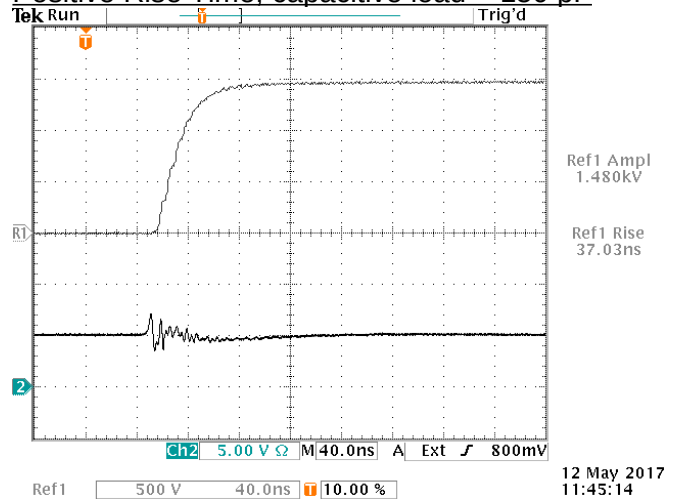


Daughterboard installed in ZIF socket, in positive position

Positive Rise Time, capacitive load = 75 pF

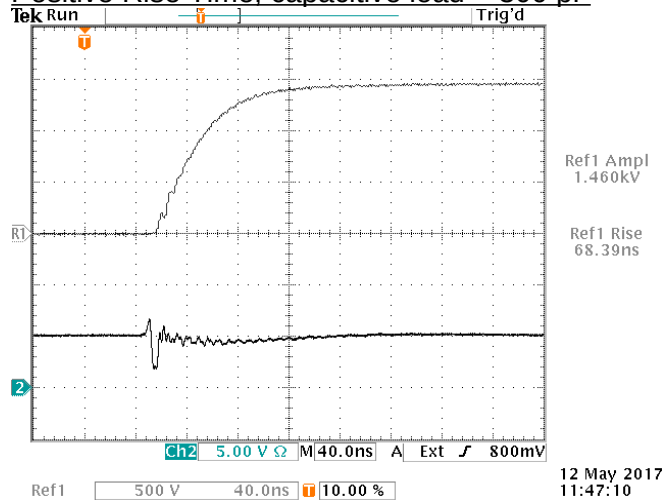


Positive Rise Time, capacitive load = 150 pF

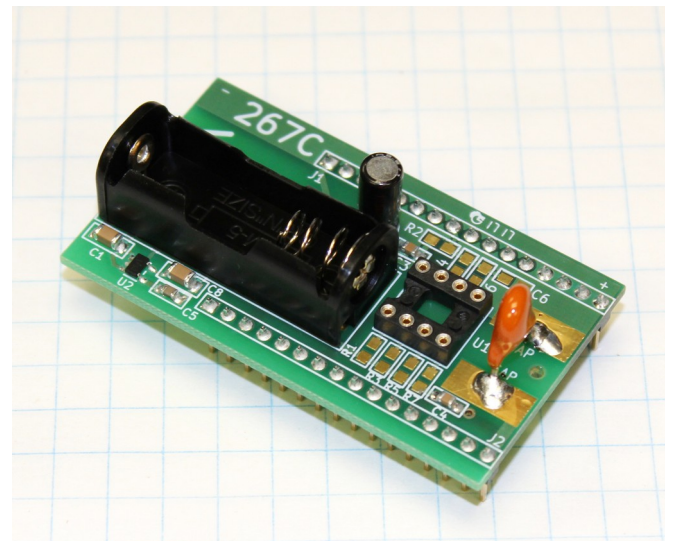
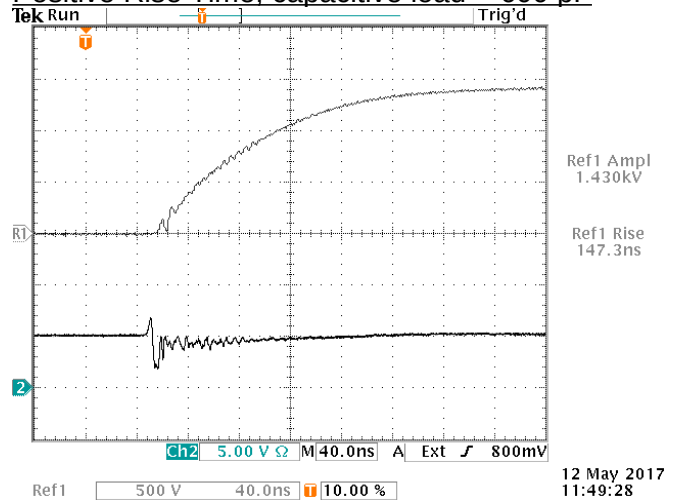


Top = HV out  
Bottom = Logic out, VCC2 = +5V, using P6246,  
and no DUT, R2 = 1 k $\Omega$

Positive Rise Time, capacitive load = 300 pF

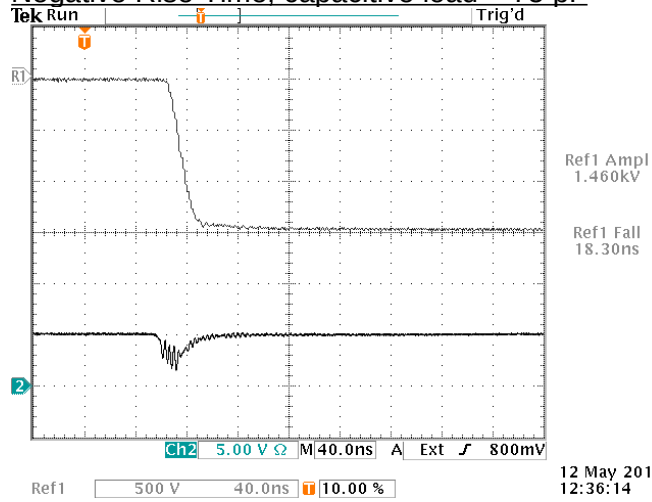


Positive Rise Time, capacitive load = 600 pF



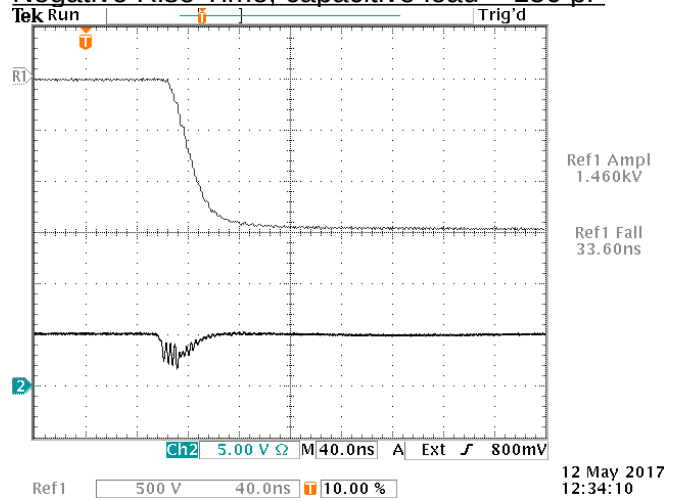
150 pF capacitor (orange) on daughterboard

Negative Rise Time, capacitive load = 75 pF



12 May 2017 12:36:14

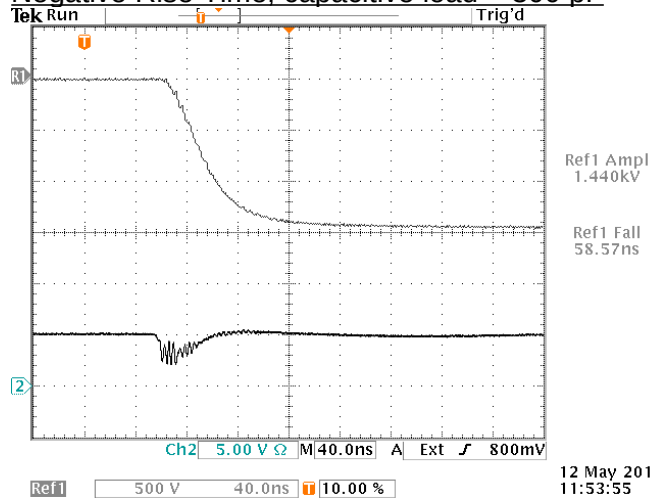
Negative Rise Time, capacitive load = 150 pF



12 May 2017 12:34:10

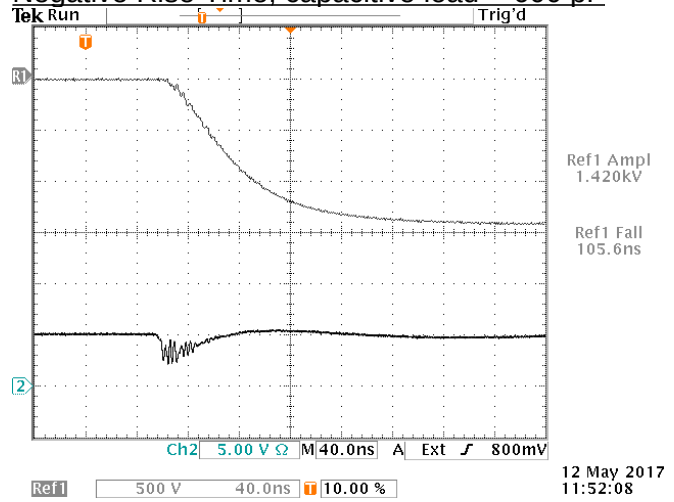
Top = HV out  
Bottom = Logic out, VCC2 = +5V, using P6246, and no DUT, R2 = 1 k $\Omega$

Negative Rise Time, capacitive load = 300 pF

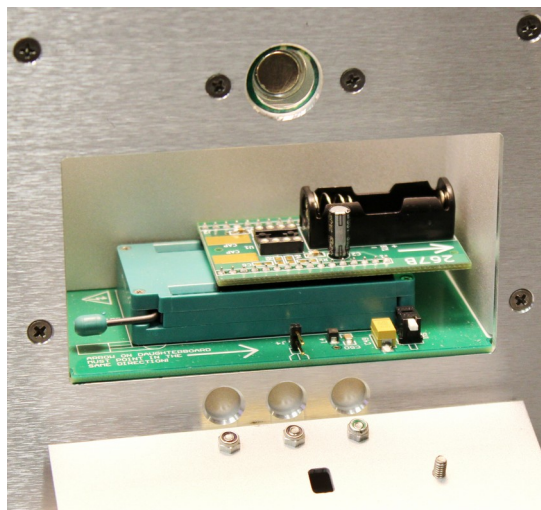


12 May 2017 11:53:55

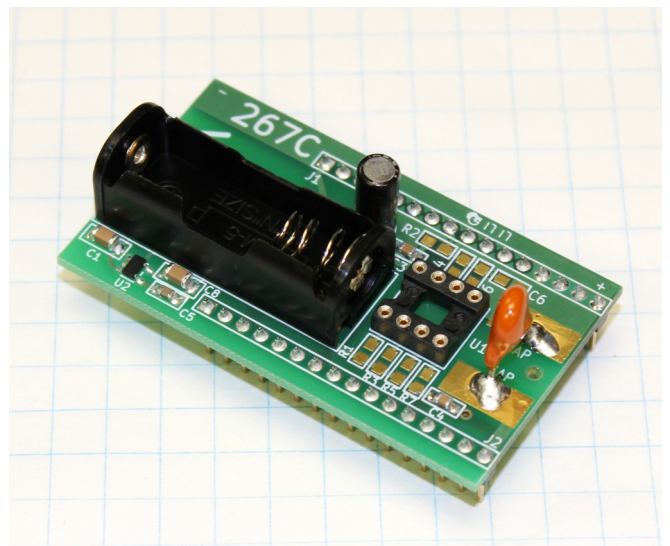
Negative Rise Time, capacitive load = 600 pF



12 May 2017 11:52:08

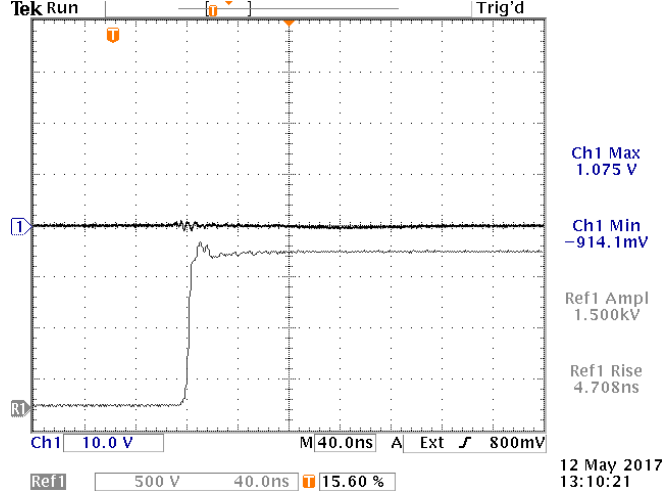


Daughterboard installed in ZIF socket, in negative position



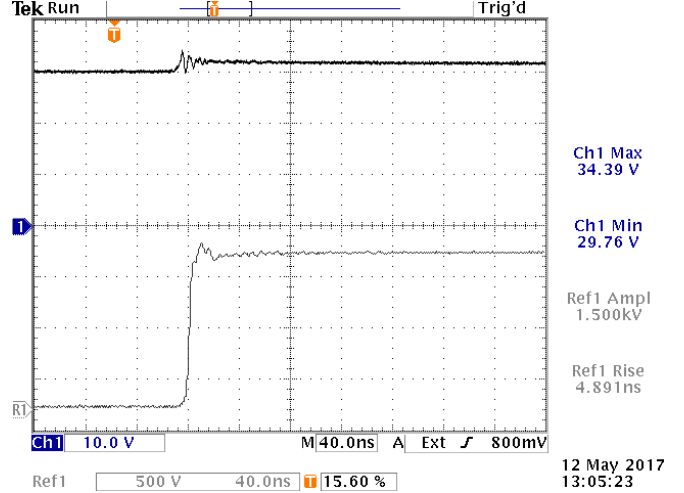
150 pF capacitor (orange) on daughterboard

VO3120 Test, 0 mA input, +1.5 kV pulse



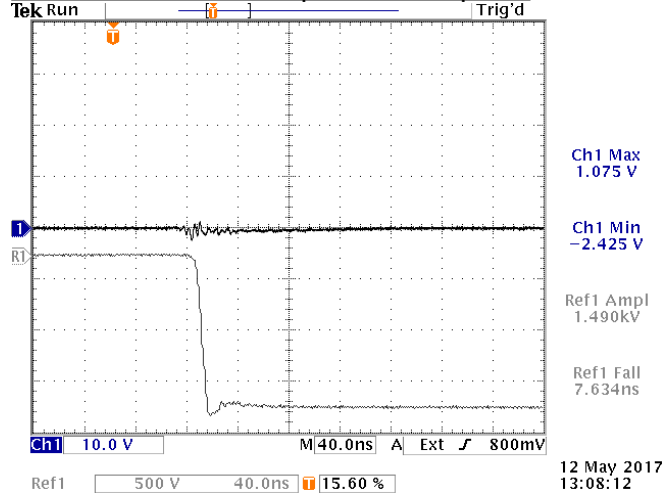
Top = Logic output (with +32V supply). No glitch.  
Bottom = high voltage pulse

VO3120 Test, 10 mA input, +1.5 kV pulse



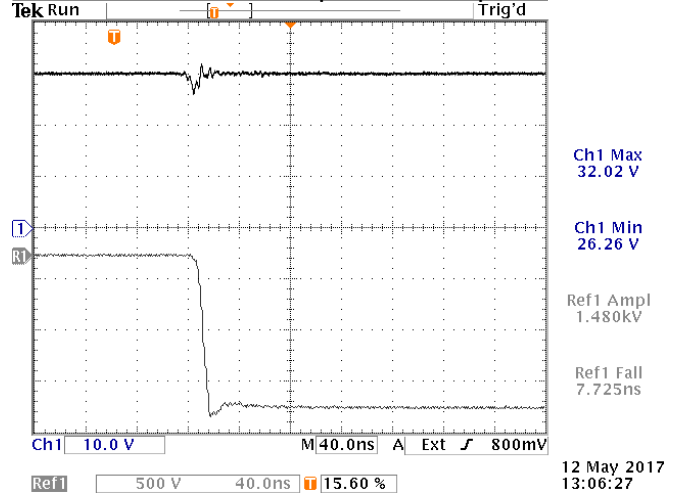
Top = Logic output (with +32V supply). No glitch.  
Bottom = high voltage pulse

VO3120 Test, 0 mA input, -1.5 kV pulse

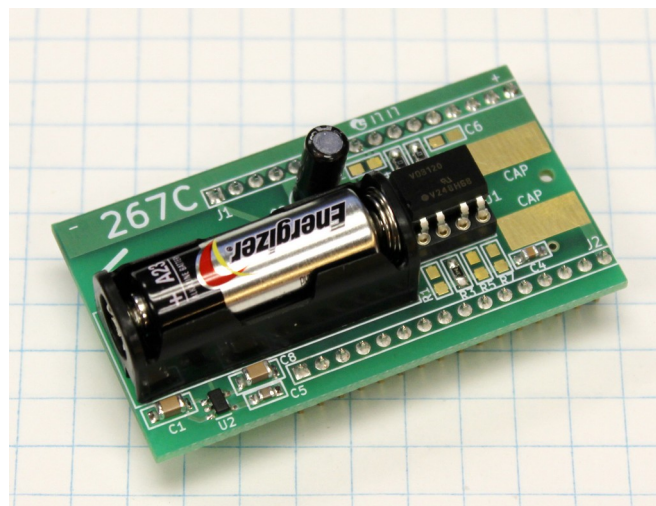


Top = Logic output (with +32V supply). No glitch.  
Bottom = high voltage pulse

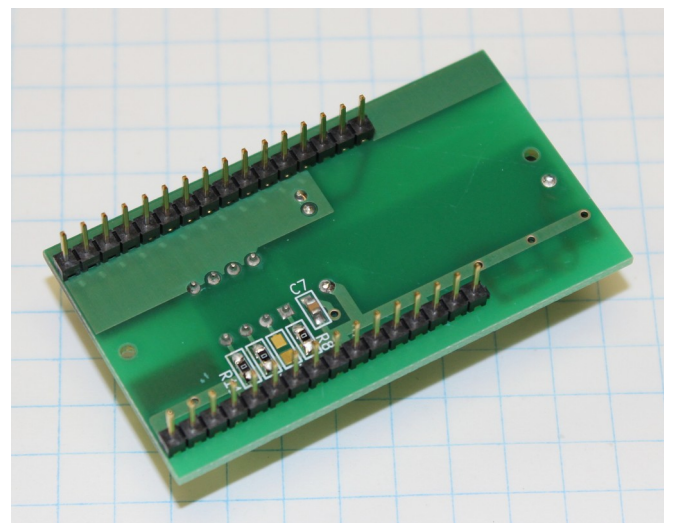
VO3120 Test, 10 mA input, -1.5 kV pulse



Top = Logic output (with +32V supply). No glitch.  
Bottom = high voltage pulse

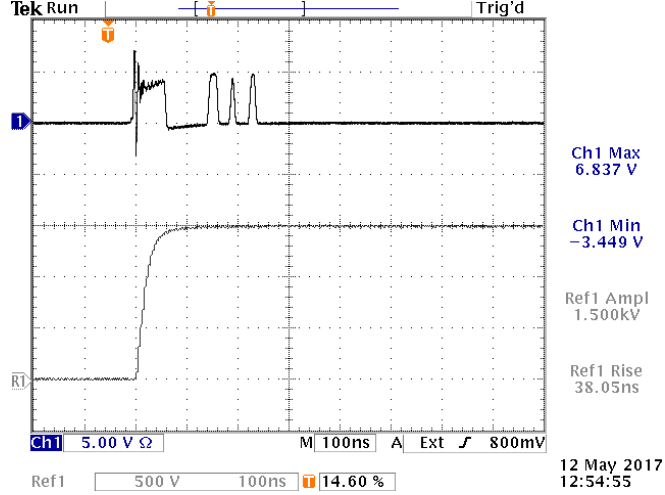


Top side of daughterboard with VO3120 configured for 10 mA bias.



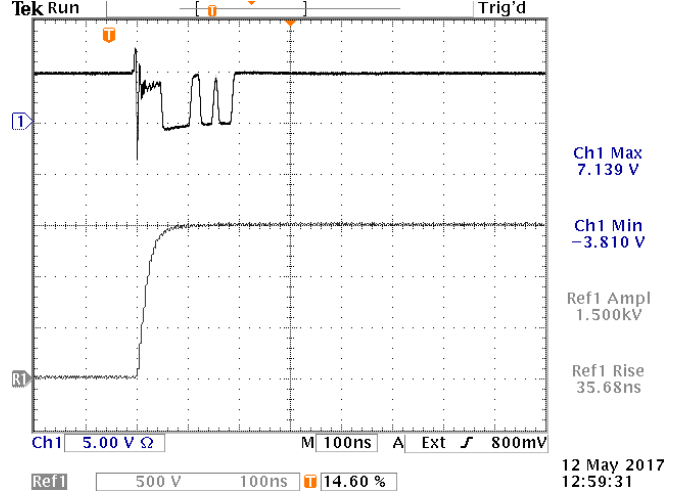
Bottom side of daughterboard with VO3120 configured for 10 mA bias.

HCPL-7721, 0V input, +1.5 kV, 150 pF added



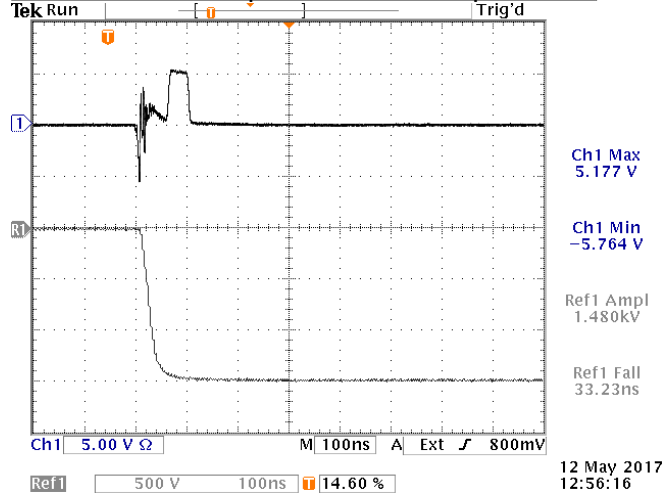
Top = Logic output (with 0V input). Glitch.  
Bottom = high voltage pulse

HCPL-7721, 5V input, +1.5 kV, 150 pF added



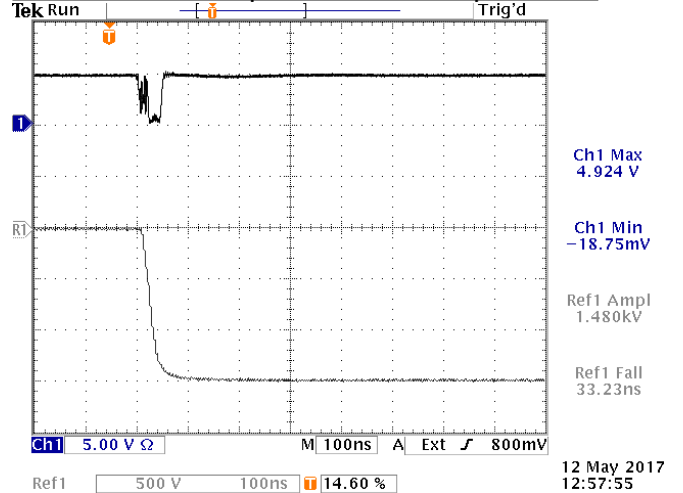
Top = Logic output (with +5V input). Glitch.  
Bottom = high voltage pulse

HCPL-7721, 0V input, -1.5 kV, 150 pF added

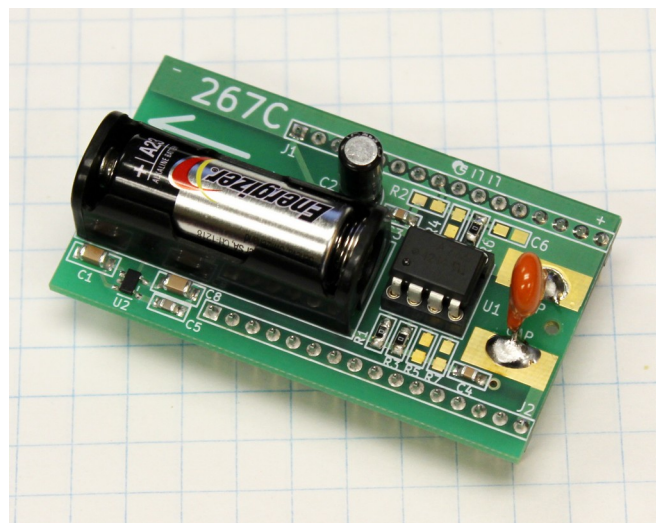


Top = Logic output (with 0V input). Glitch.  
Bottom = high voltage pulse

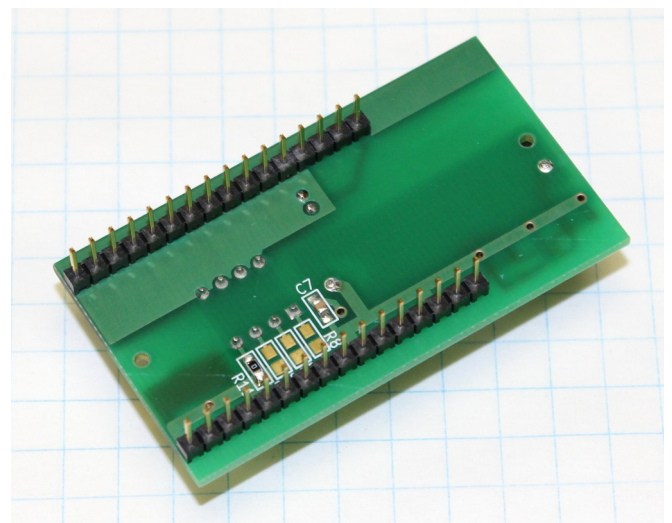
HCPL-7721, 5V input, -1.5 kV, 150 pF added



Top = Logic output (with +5V input). Glitch.  
Bottom = high voltage pulse



Top side of daughterboard with HCPL-7721 configured for 5V bias.



Bottom side of daughterboard with HCPL-7721 configured for 5V bias.