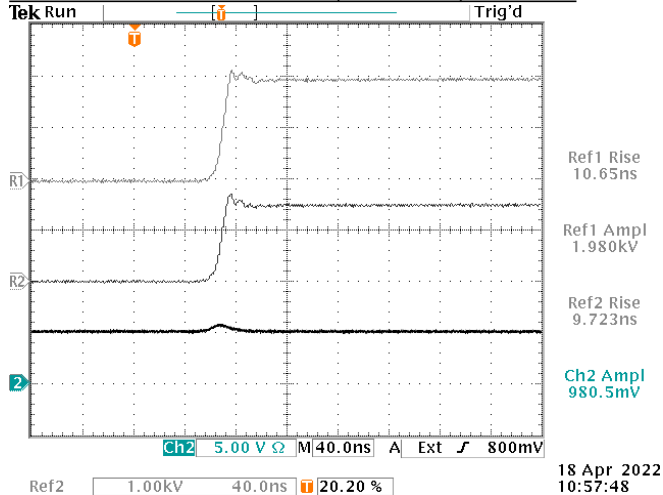


PERFORMANCE CHECKSHEET

Model: AVRQ-5-B-AHV-HF-FPD-V2-ATA3-AC22  
 Type: Common Mode Transient Immunity (CMTI) Test for Opto-Couplers  
 S.N.: 14229  
 Date: April 18, 2022

Minimum Rise Time Test, No DUT, Positive



a) Output Signal Amplitude:  $\pm 1.5$  to  $\pm 2$  kV

b) Rise Time (10%-90%):  $< 15$  to  $> 50$  ns

c) PRF: 1 Hz - 100 Hz

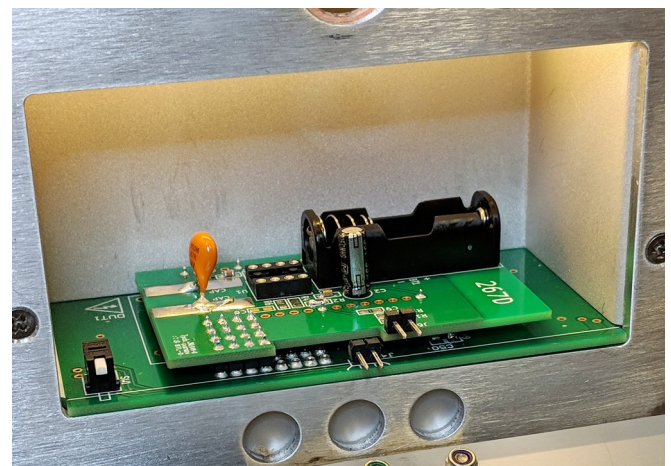
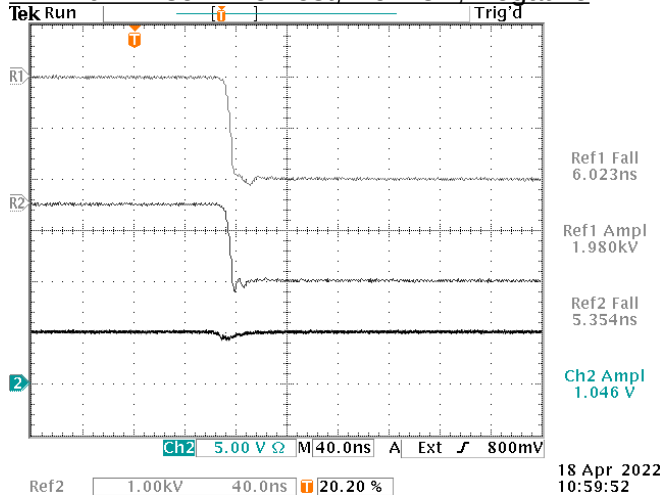
d) Jitter, Stability: OK

e) Prime Power: 100-240V AC, 50-60 Hz.

Top = +1.5 and +2.0 kV HV out (stored - with signal disconnected before recording logic waveform).

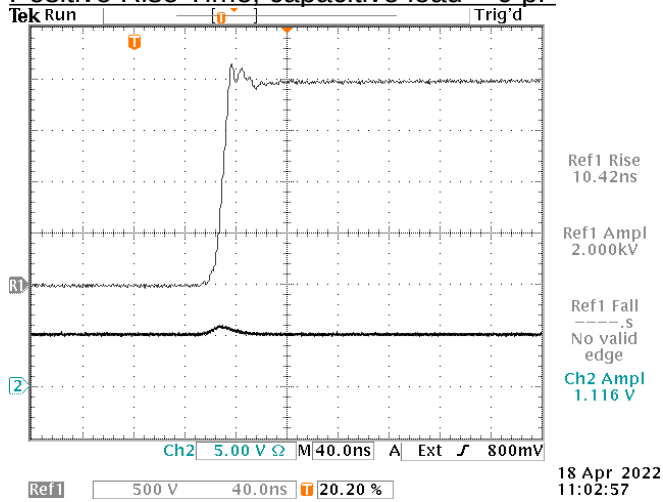
Bottom = Logic "A" out for +1.5 kV, VCC2 = +5V, using P6246, and no DUT, R2 = 1 k $\Omega$ . (This shows the parasitic capacitive coupling onto the Logic "A" out.)

Minimum Rise Time Test, No DUT, Negative

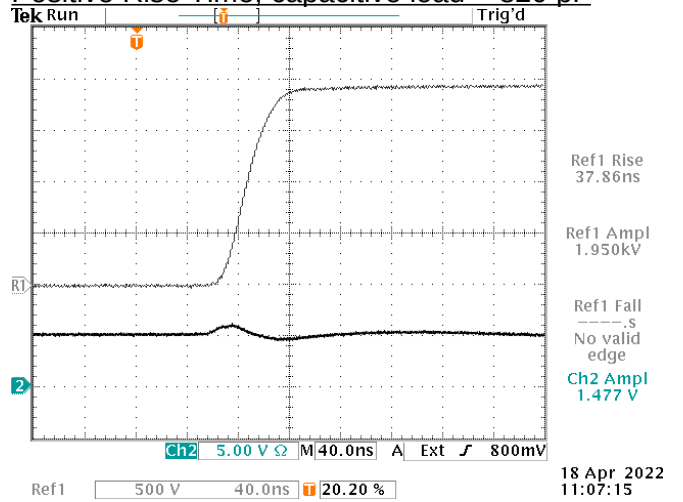


Daughterboard installed in positive position (with no DUT IC)

Positive Rise Time, capacitive load = 0 pF

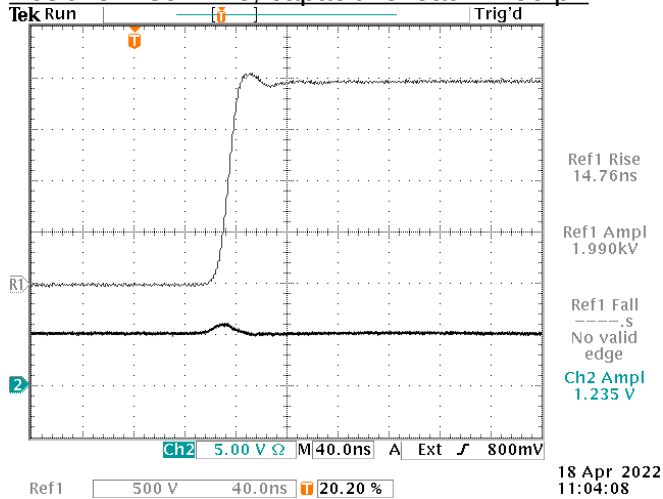


Positive Rise Time, capacitive load = 820 pF

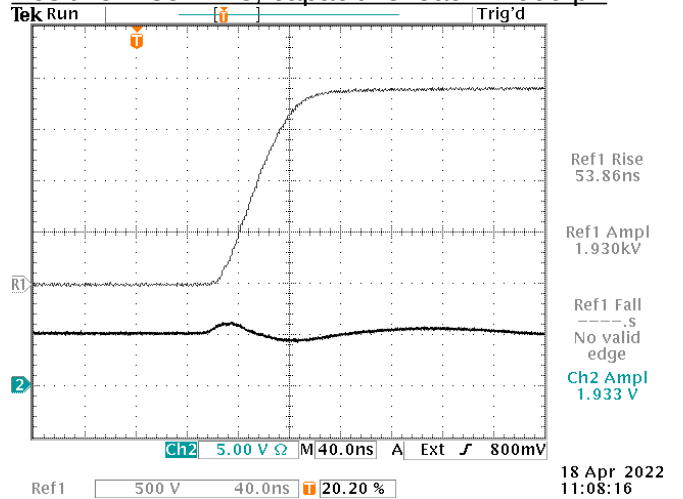


Top = HV out (stored - with signal disconnected before recording logic waveform)  
 Bottom = Logic "A" out, VCC2 = +5V, using P6246 probe, and no DUT, R2 = 1 kΩ

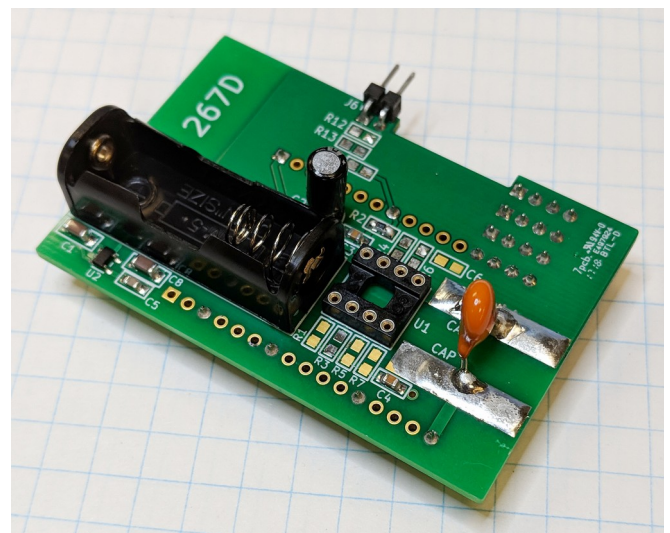
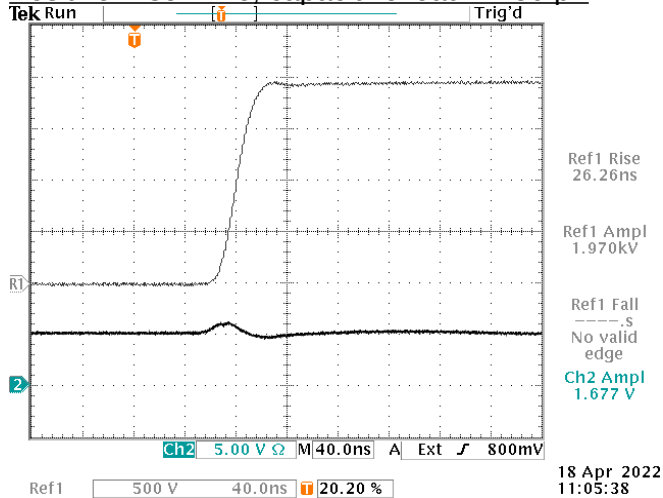
Positive Rise Time, capacitive load = 150 pF



Positive Rise Time, capacitive load = 1000 pF

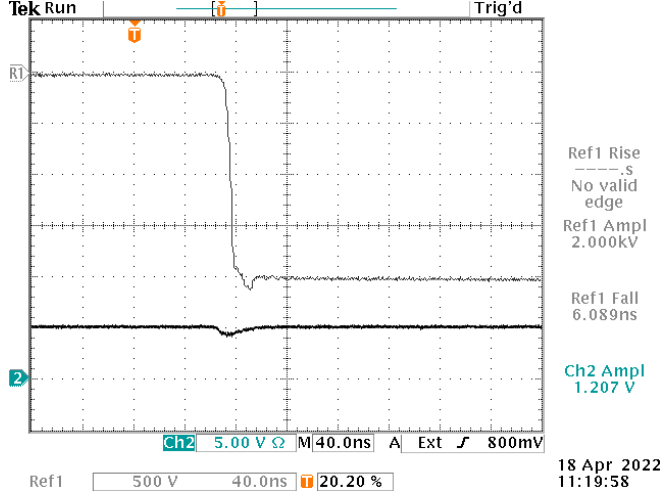


Positive Rise Time, capacitive load = 450 pF

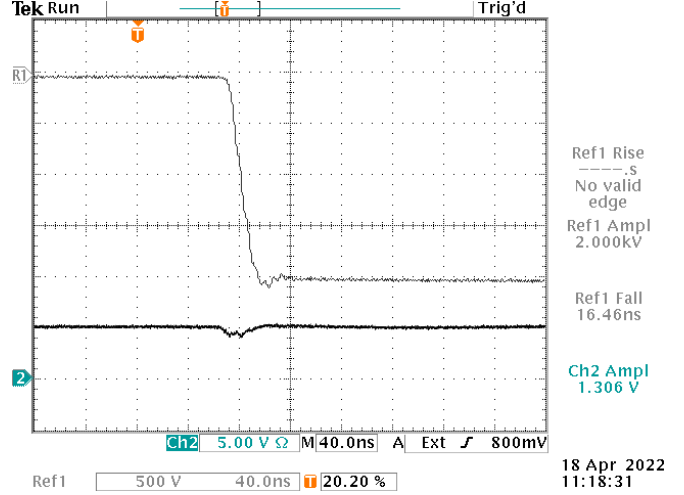


150 pF capacitor (orange) on daughterboard

Negative Rise Time, capacitive load = 0 pF

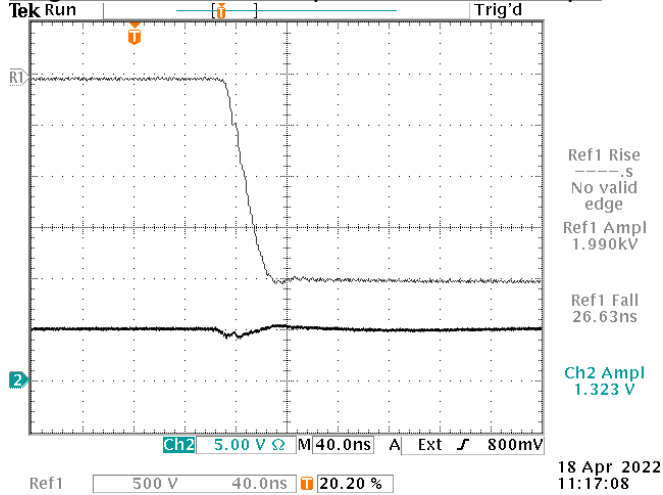


Negative Rise Time, capacitive load = 150 pF

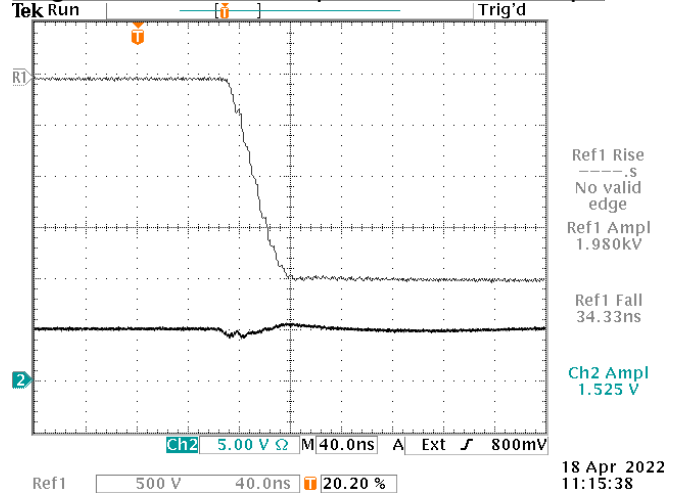


Top = HV out (stored - with signal disconnected before recording logic waveform)  
 Bottom = Logic "A" out, VCC2 = +5V, using P6246 probe, and no DUT, R2 = 1 kΩ

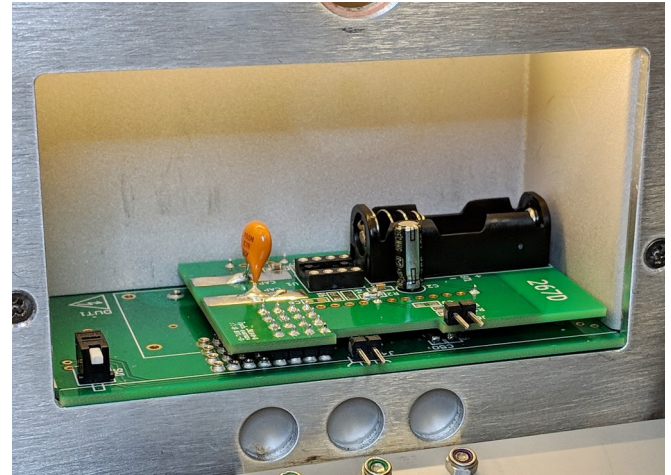
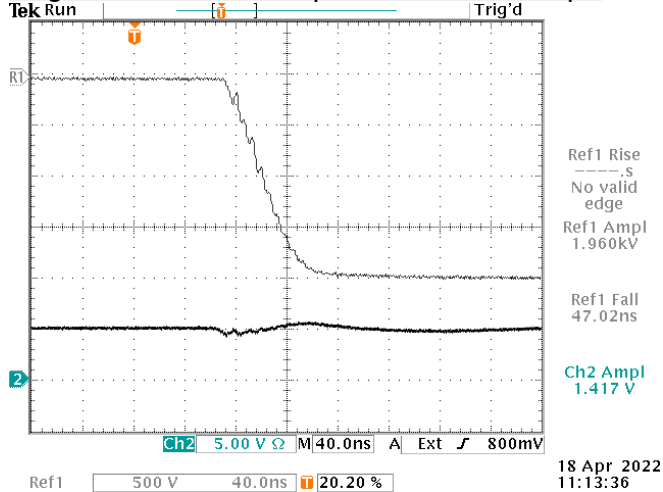
Negative Rise Time, capacitive load = 300 pF



Negative Rise Time, capacitive load = 450 pF

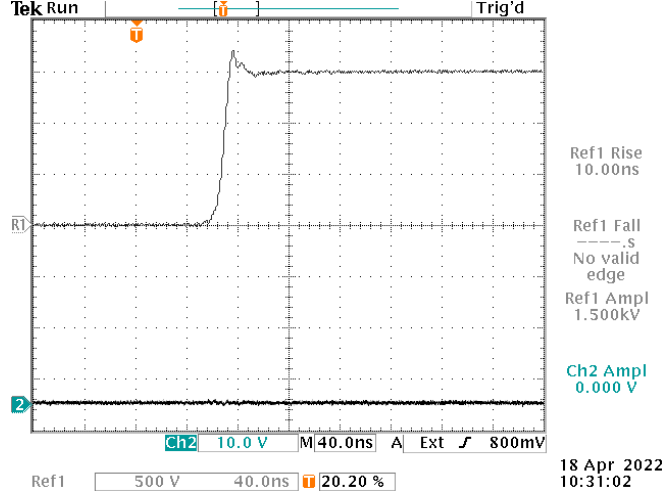


Negative Rise Time, capacitive load = 820 pF

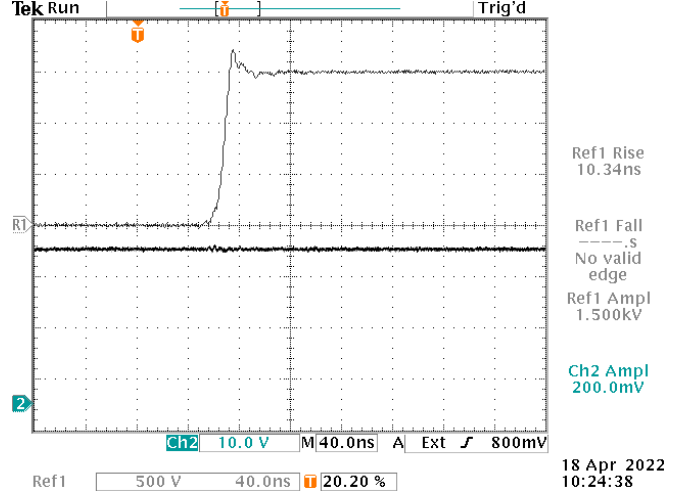


Daughterboard installed in negative position (with no DUT IC)

MPC50 #2 Test, 0 mA input, +1.5 kV pulse

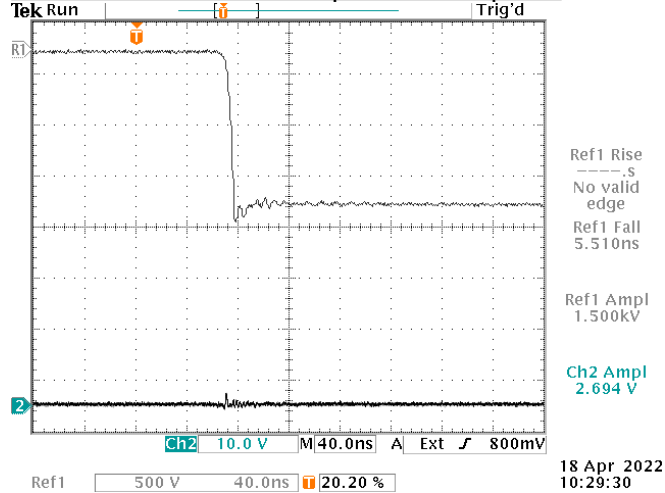


MPC50 #2 Test, 10 mA input, +1.5 kV pulse

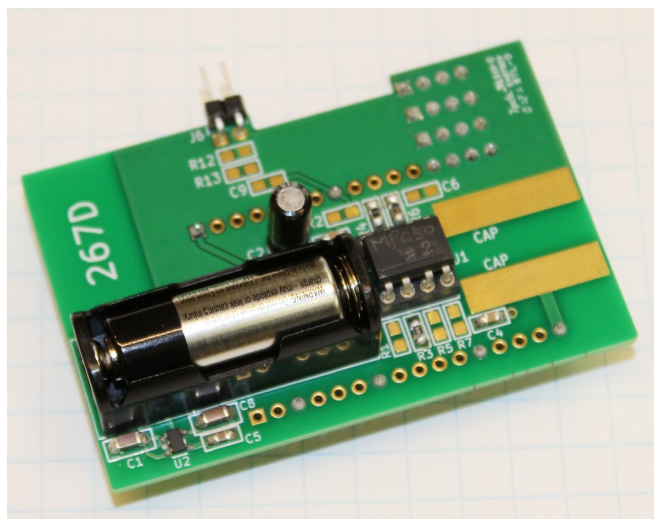
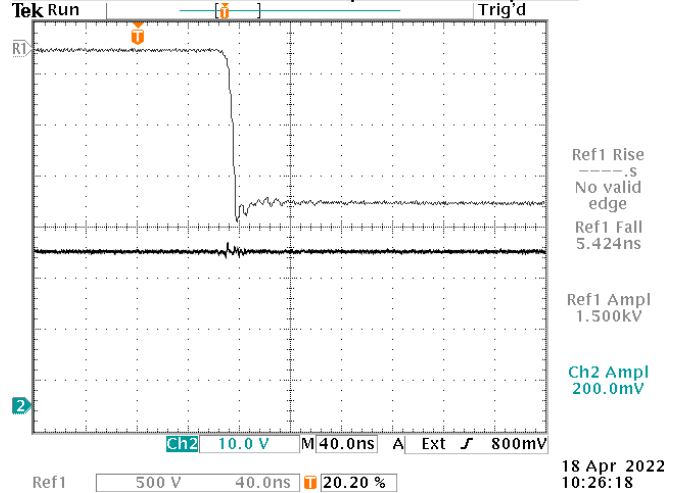


Top = HV out (stored - with signal disconnected before recording logic waveform)  
 Bot = Logic "A" out, +30V VCC2. P6139A probe.

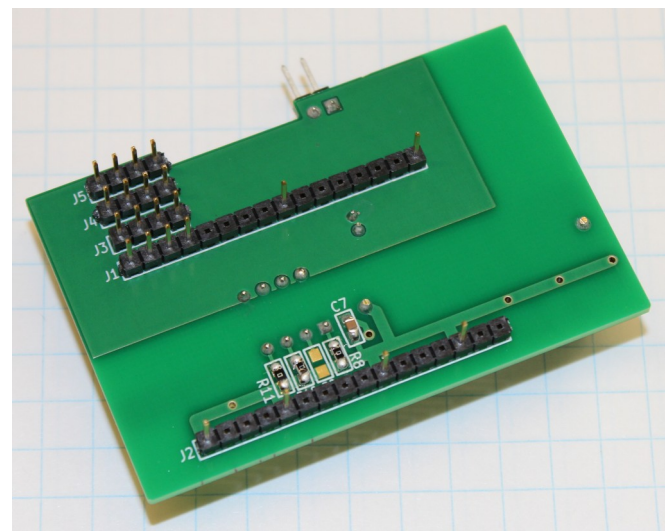
MPC50 #2 Test, 0 mA input, -1.5 kV pulse



MPC50 #2 Test, 10 mA input, -1.5 kV pulse

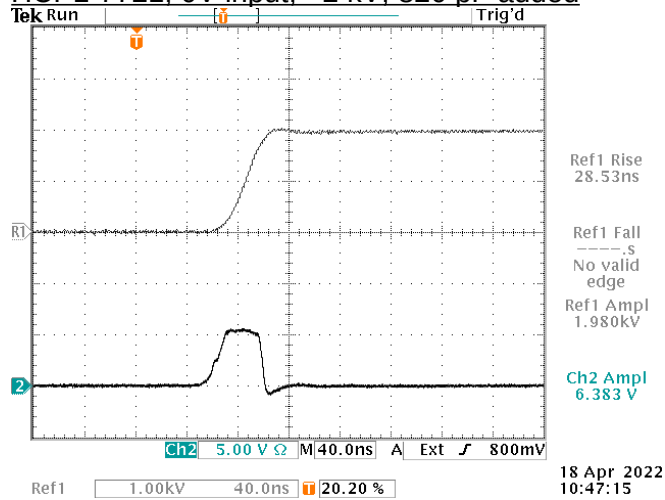


Top side of daughterboard with MPC50 #2 configured for 10 mA bias.

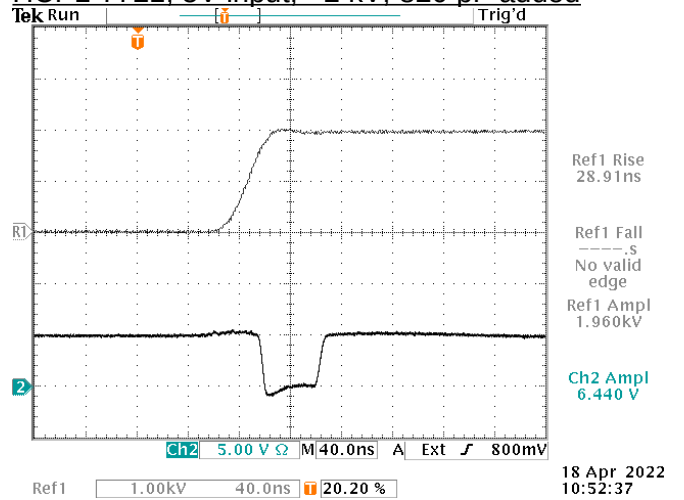


Bottom side of daughterboard with MPC50 #2 configured for 10 mA bias.

### HCPL-7721, 0V input, +2 kV, 820 pF added

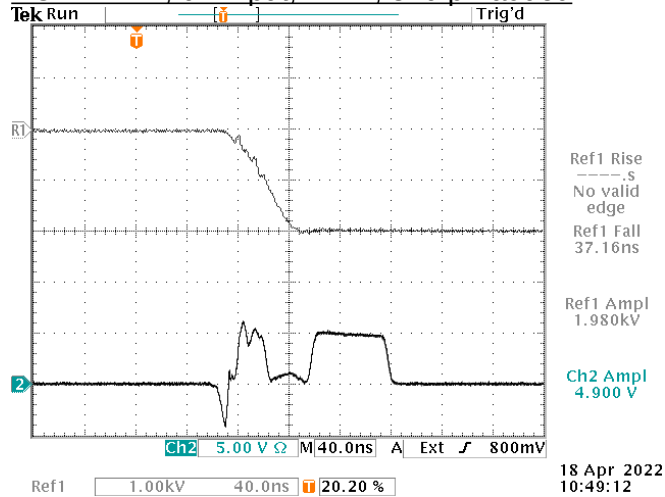


### HCPL-7721, 5V input, +2 kV, 820 pF added

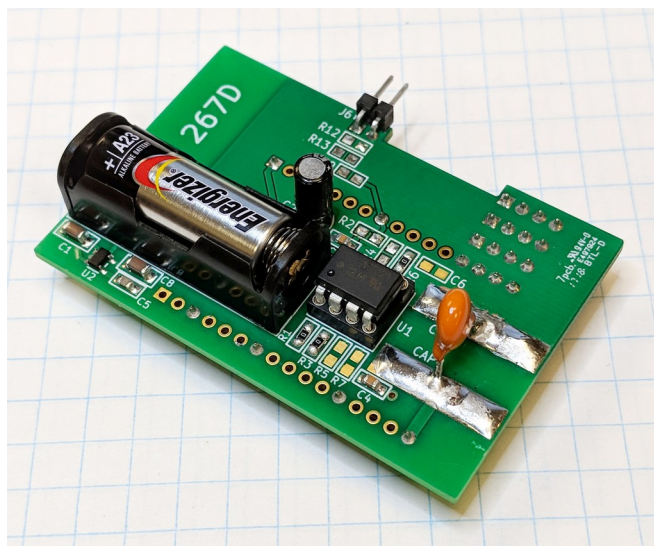
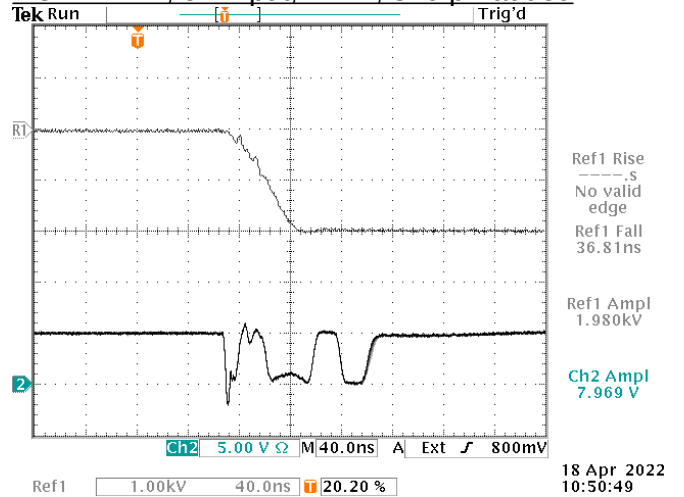


Top = high voltage pulse (stored - with signal disconnected before recording logic waveform).  
 Bot = Logic "A" out (with 0V input) using P6246.

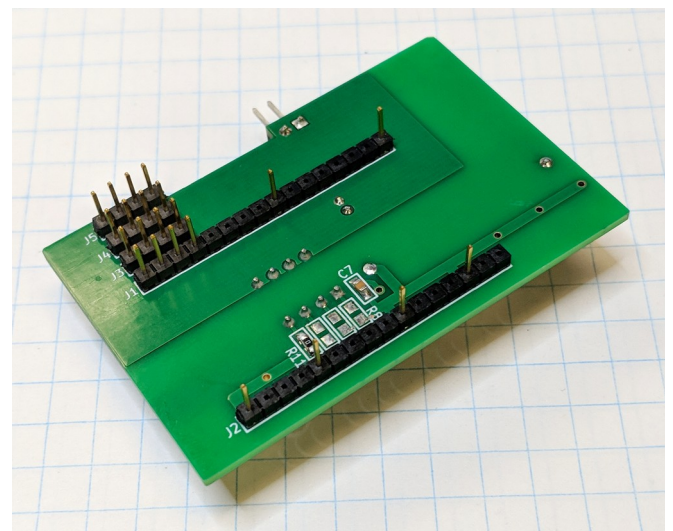
### HCPL-7721, 0V input, -2 kV, 820 pF added



### HCPL-7721, 5V input, -2 kV, 820 pF added



Top side of daughterboard with HCPL-7721 configured for 5V bias.



Bottom side of daughterboard with HCPL-7721 configured for 5V bias.