AVTECH ELECTROSYSTEMS LTD.
NANOSECOND WAVEFORM ELECTRONICS
SINCE 1975

info@avtechpulse.com
http://www.avtechpulse.com/

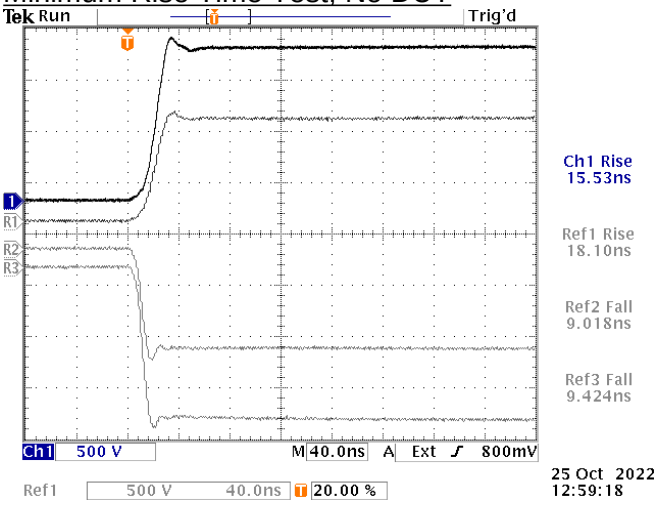
Tel: 888-670-8729 (USA & Canada)
or +1-613-686-6675 (Worldwide)

BOX 5120, LCD MERIVALE
OTTAWA, CANADA K2C3H5

PERFORMANCE CHECKSHEET

Model: AVRQ-4-B-AHV-FPD-SCHB-AC03-ATA3-HF
Type: Common Mode Transient Immunity (CMTI) Pulser for Opto-Coupler Tests
S.N.: 14270 (modified)
Date: October 25, 2022

Minimum Rise Time Test, No DUT



+1.5 kV, +1.0 kV, -1.0 kV, and -1.5 kV with minimum rise time setting

a) Output Signal Amplitude: ±1.0 to ±1.5 kV

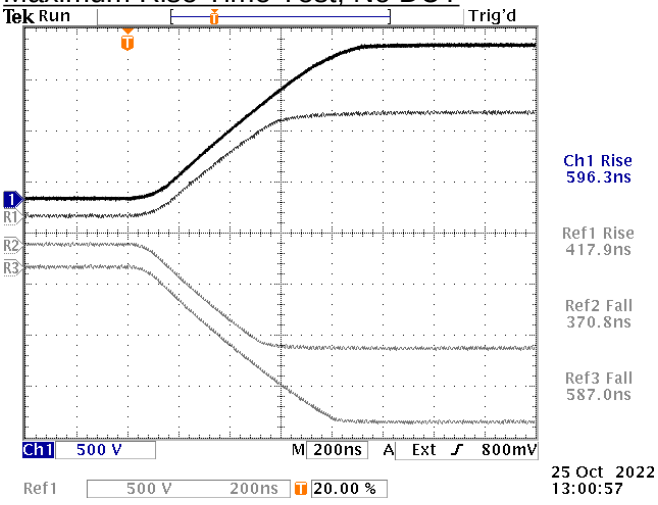
b) Rise Time (10%-90%): < 20 to > 500 ns

c) PRF: 1 Hz - 100 Hz

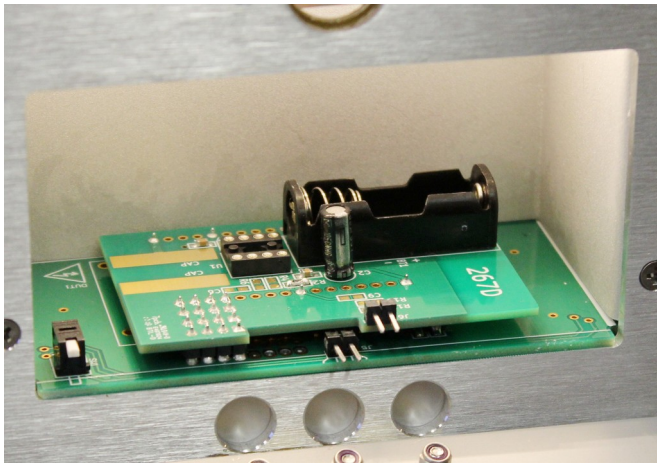
d) Jitter, Stability: OK

e) Prime Power: 100-240V AC, 50-60 Hz.

Maximum Rise Time Test, No DUT

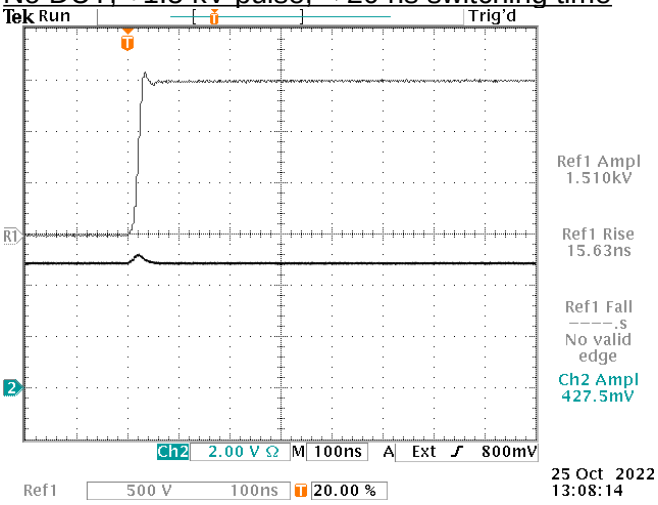


+1.5 kV, +1.0 kV, -1.0 kV, and -1.5 kV with maximum rise time setting

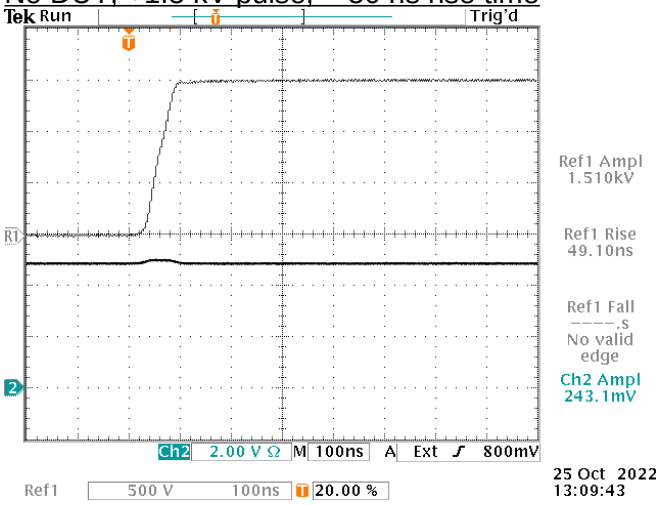


Daughterboard installed
(with no DUT IC)

No DUT, +1.5 kV pulse, < 20 ns switching time

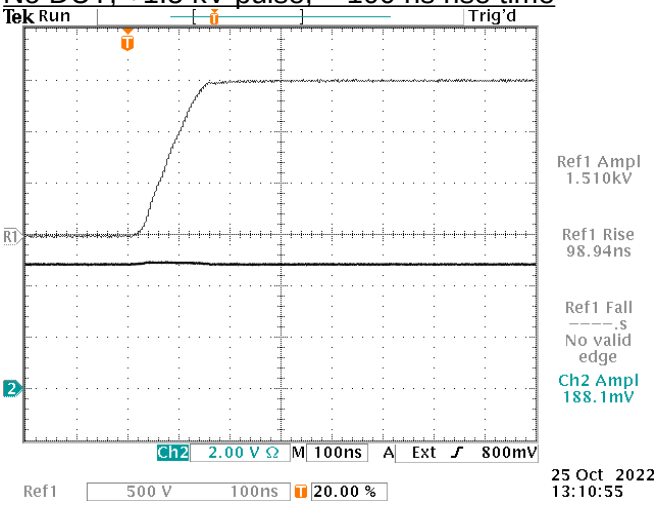


No DUT, +1.5 kV pulse, ~ 50 ns rise time

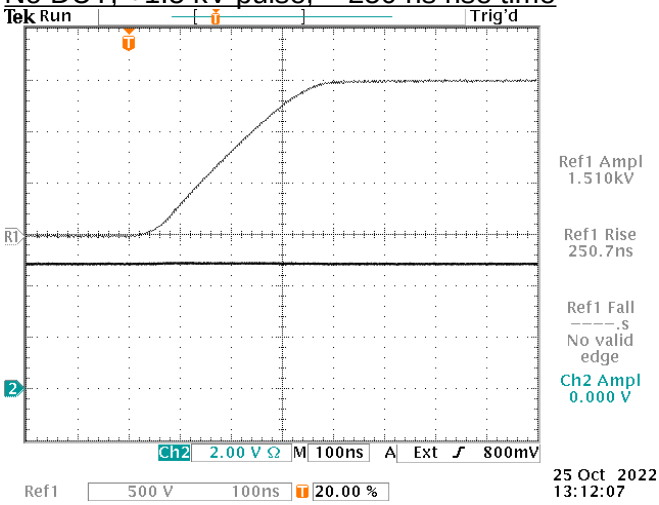


Top = HV out (stored - with signal disconnected before recording logic waveform)
Bottom = Logic out “A” of a standard PCB 267D daughterboard, VCC2 = +5V, using P6246 probe, and no DUT, R2 = 1 kΩ

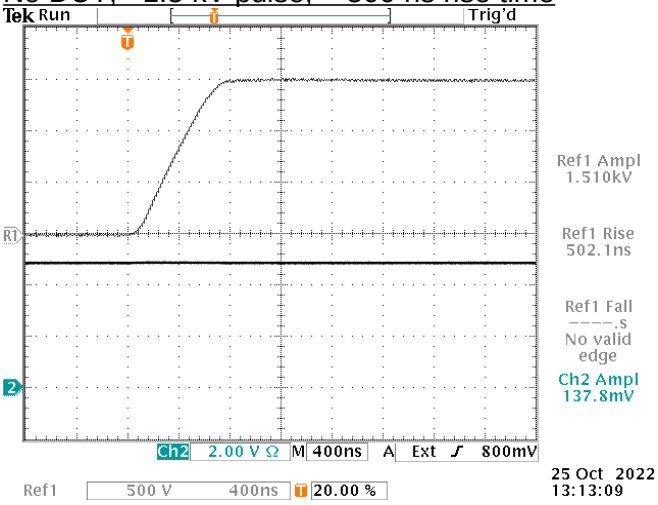
No DUT, +1.5 kV pulse, ~ 100 ns rise time



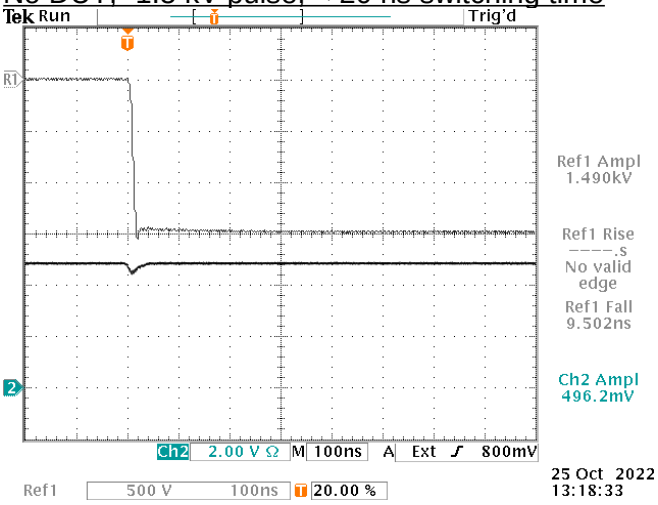
No DUT, +1.5 kV pulse, ~ 250 ns rise time



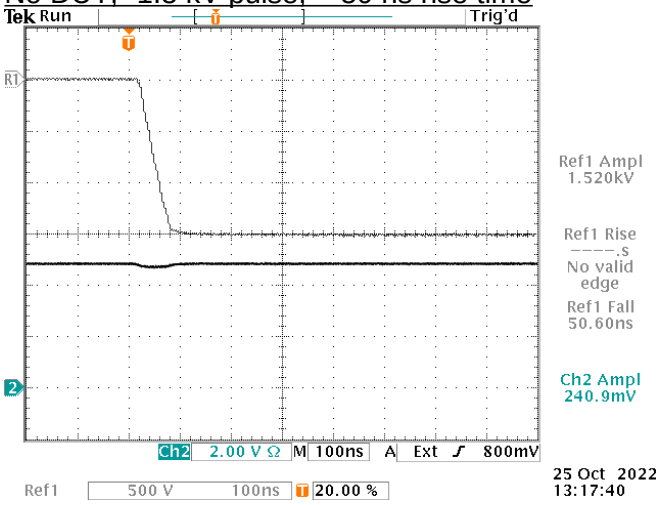
No DUT, +1.5 kV pulse, ~ 500 ns rise time



No DUT, -1.5 kV pulse, < 20 ns switching time

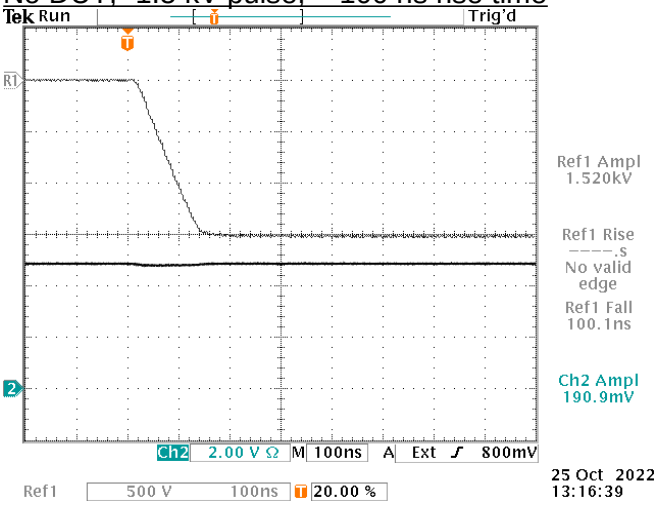


No DUT, -1.5 kV pulse, ~ 50 ns rise time

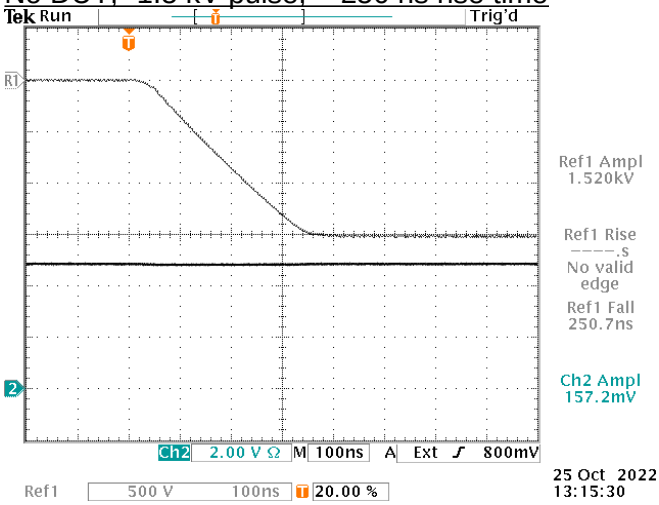


Top = HV out (stored - with signal disconnected before recording logic waveform)
Bottom = Logic out “A” of a standard PCB 267D daughterboard, VCC2 = +5V, using P6246 probe, and no DUT, R2 = 1 kΩ

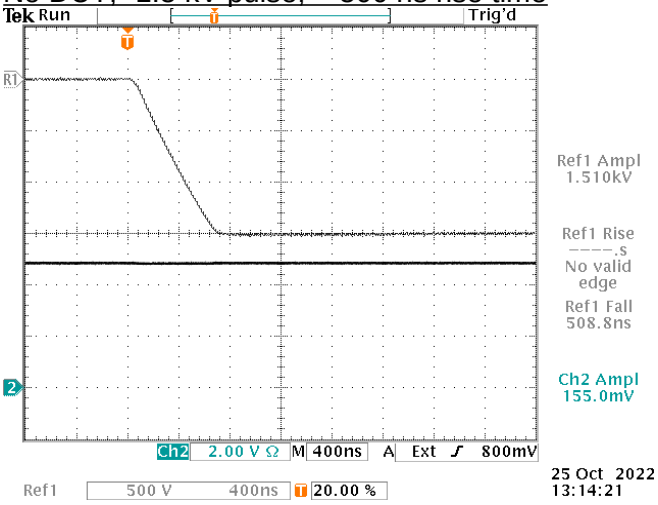
No DUT, -1.5 kV pulse, ~ 100 ns rise time



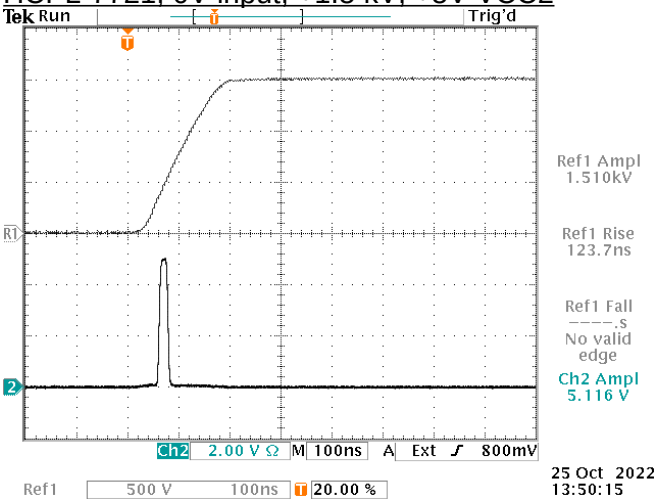
No DUT, -1.5 kV pulse, ~ 250 ns rise time



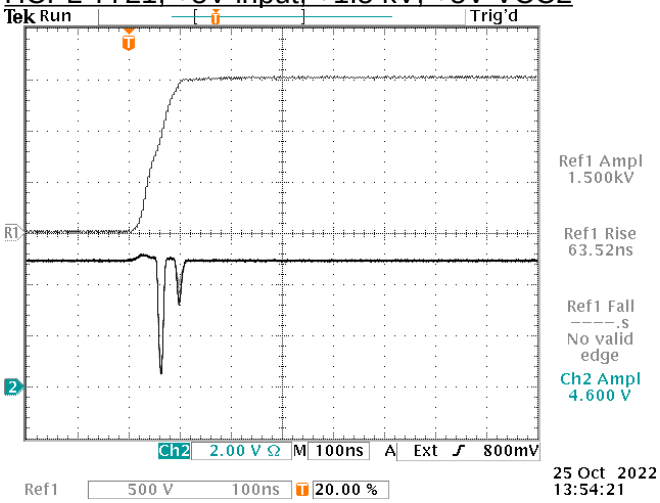
No DUT, -1.5 kV pulse, ~ 500 ns rise time



HCPL-7721, 0V input, +1.5 kV, +5V VCC2

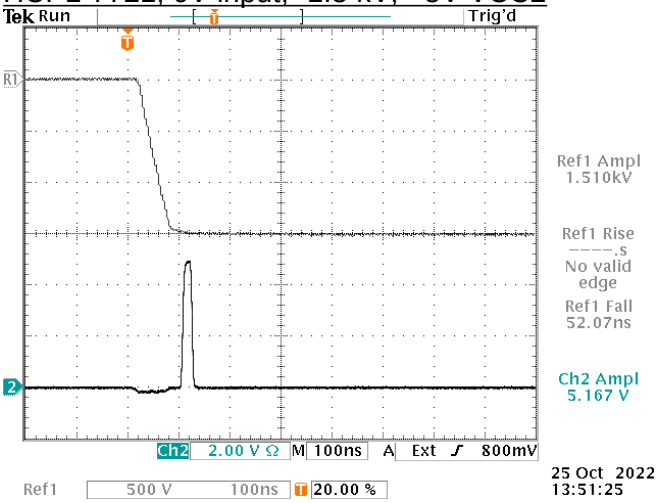


HCPL-7721, +5V input, +1.5 kV, +5V VCC2

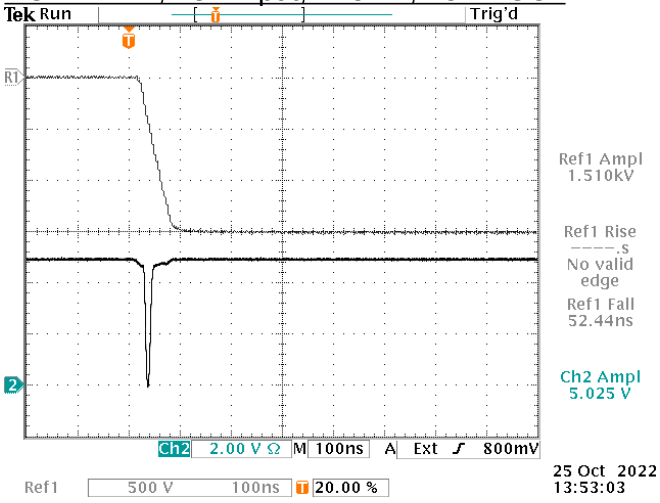


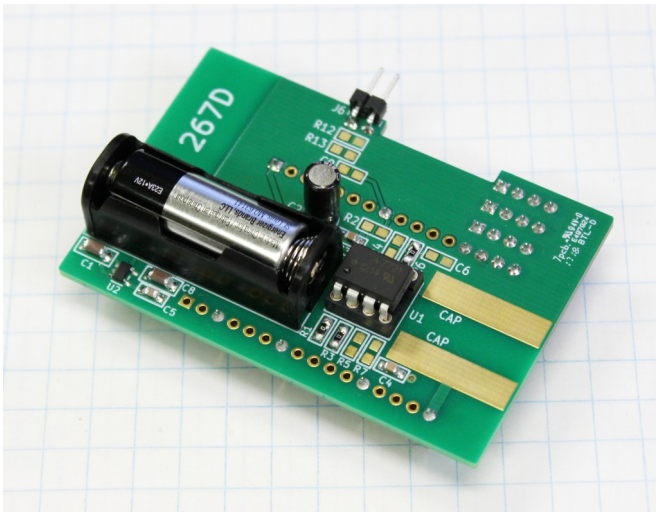
Top = high voltage pulse
Bottom = Logic output

HCPL-7721, 0V input, -1.5 kV, +5V VCC2

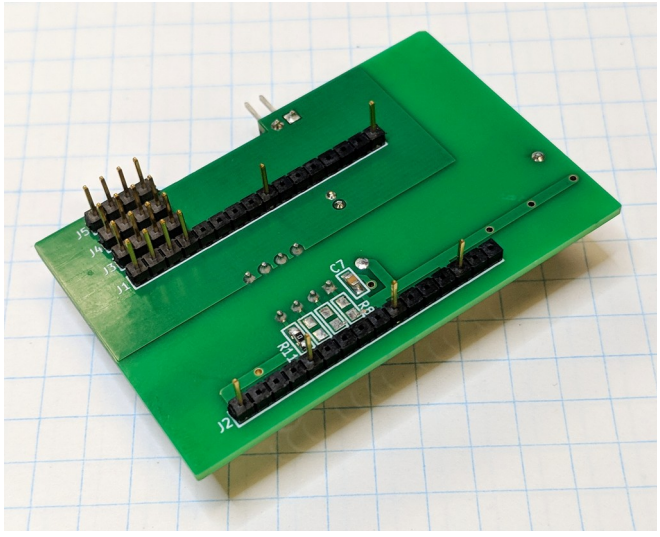


HCPL-7721, +5V input, -1.5 kV, +5V VCC2



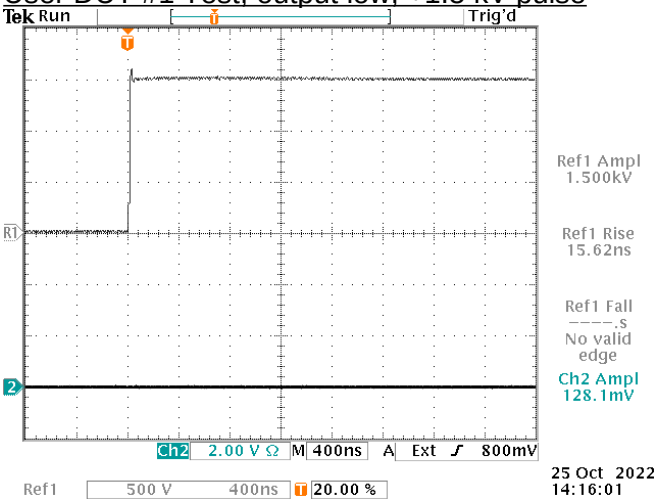


Top side of daughterboard with HCPL-7721 configured for 5V bias.



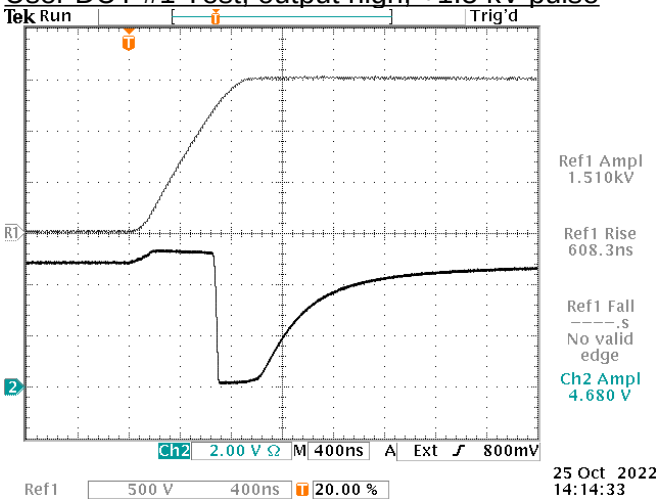
Bottom side of daughterboard with HCPL-7721 configured for 5V bias.

User DUT #1 Test, output low, +1.5 kV pulse



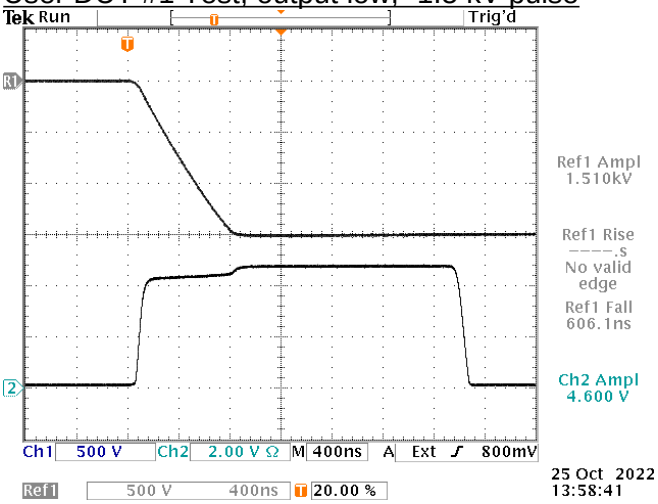
No glitch observed for any rise time setting.

User DUT #1 Test, output high, +1.5 kV pulse



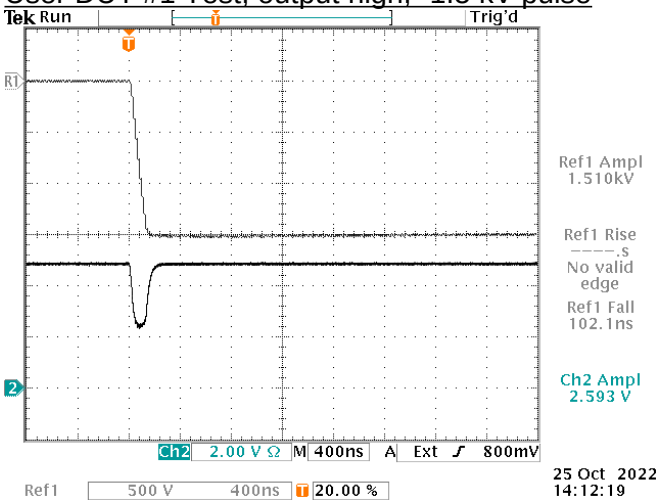
Glitch observed even at maximum rise time.

User DUT #1 Test, output low, -1.5 kV pulse

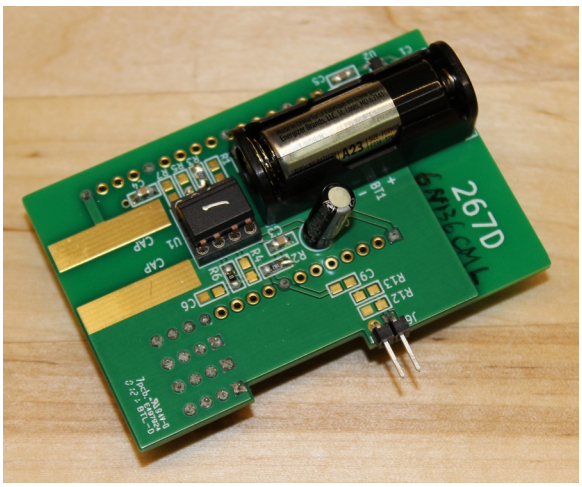


Glitch observed even at maximum rise time.

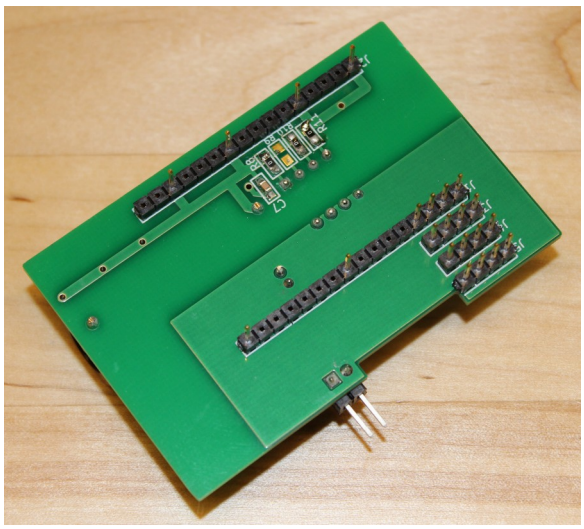
User DUT #1 Test, output high, -1.5 kV pulse



> 50% glitch observed for t_R < 102.1 ns

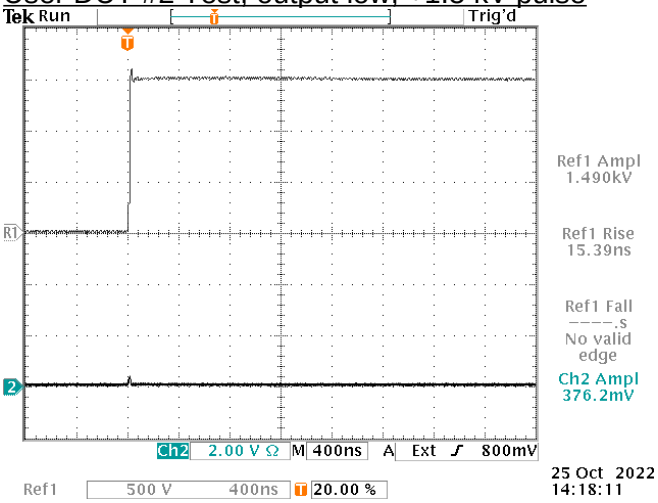


Top side of user's daughterboard with DUT #1 configured with R3 = 220Ω (IF = 16.4 mA), R2 = 1.8 kΩ (pull-up), and R6, R8, R10, R11 = 0Ω.



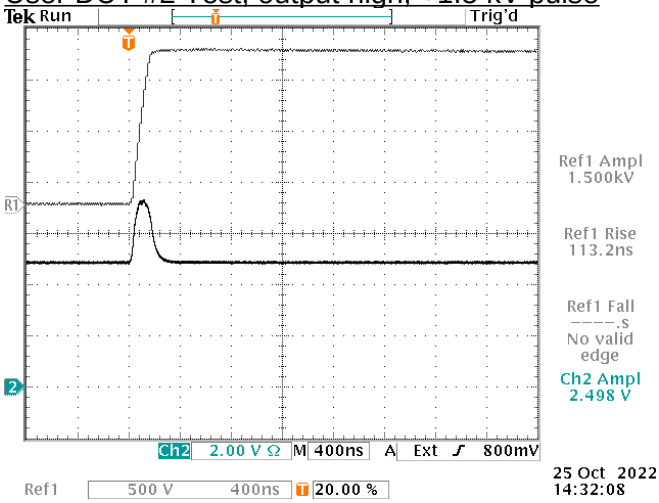
Bottom side of the same daughterboard.

User DUT #2 Test, output low, +1.5 kV pulse



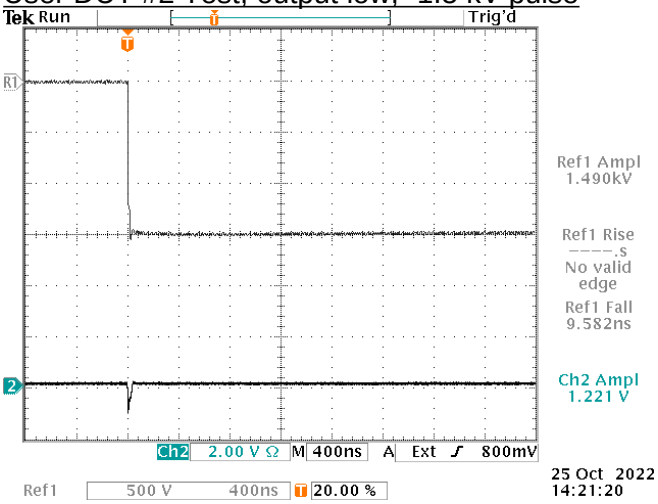
No > 50% glitch observed for any setting.

User DUT #2 Test, output high, +1.5 kV pulse



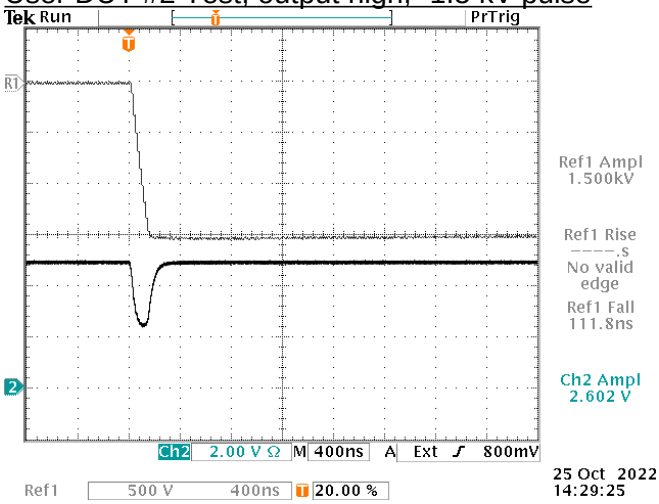
> 50% glitch observed for t_R < 113.2 ns

User DUT #2 Test, output low, -1.5 kV pulse

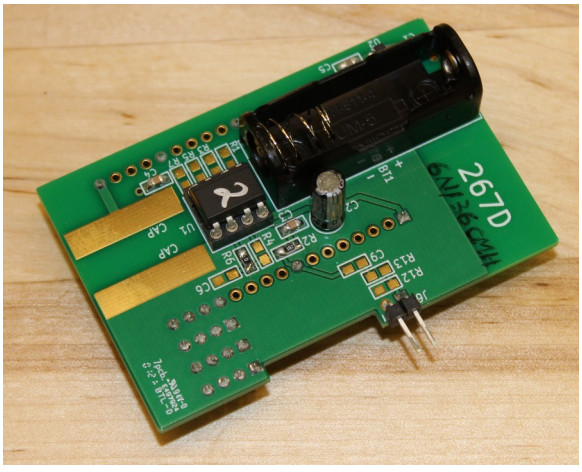


No > 50% glitch observed for any setting.

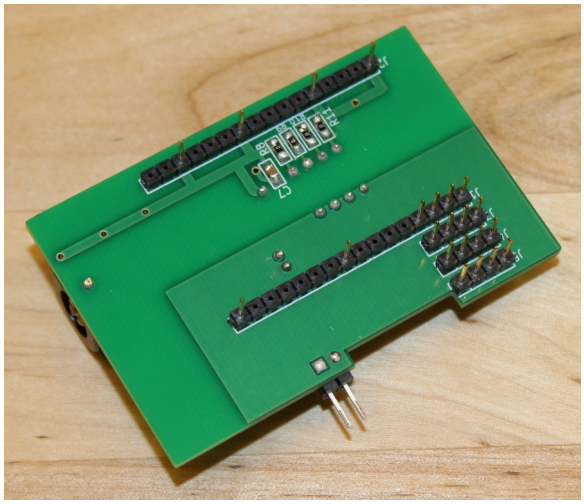
User DUT #2 Test, output high, -1.5 kV pulse



> 50% glitch observed for t_R < 111.8 ns



Top side of user's daughterboard with DUT #2 configured with R9 = 0Ω (IF = 0 mA), R2 = 1.8 kΩ (pull-up), and R6, R8, R10, R11 = 0Ω.



Bottom side of the same daughterboard.