AVTECH ELECTROSYSTEMS LTD.
NANOSECOND WAVEFORM ELECTRONICS
SINCE 1975

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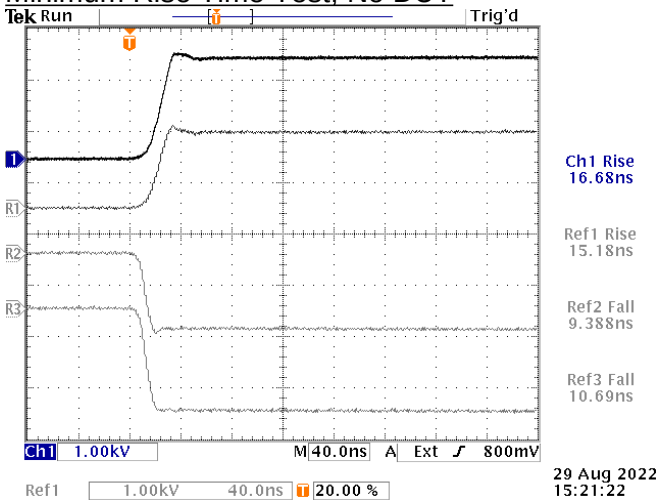
BOX 5120, LCD MERIVALE
OTTAWA, CANADA K2C3H5

PERFORMANCE CHECKSHEET

Model: AVRQ-4-B-XHV-FPD-SCHB-AC03-ATA3-HF
Type: Common Mode Transient Immunity (CMTI) Pulser for Opto-Coupler Tests
S.N.: 14270
Date: August 29, 2022

Minimum Rise Time Test, No DUT



+2 kV, +1.5 kV, -1.5 kV, and -2 kV with minimum rise time setting (1 kV/div, 40 ns/div)

a) Output Signal Amplitude: ±1.5 to ±2 kV

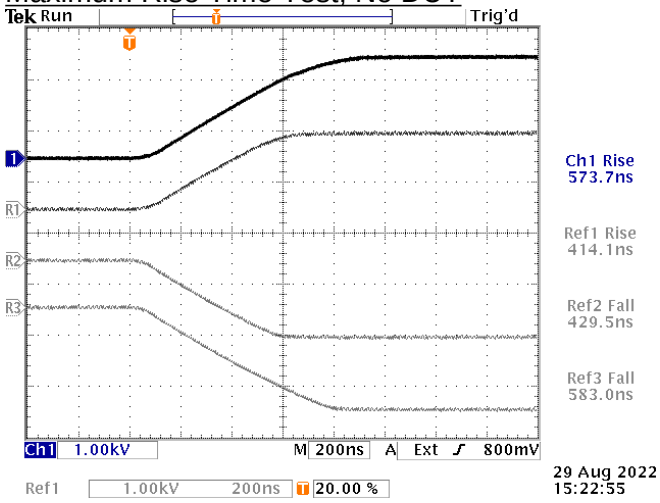
b) Rise Time (10%-90%): < 25 to > 500 ns

c) PRF: 1 Hz - 100 Hz

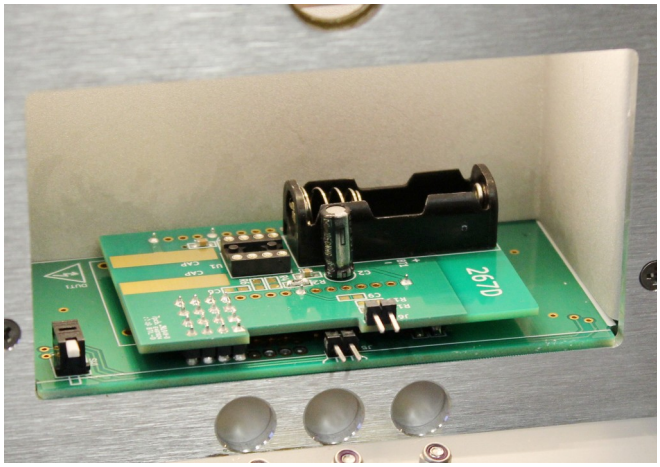
d) Jitter, Stability: OK

e) Prime Power: 100-240V AC, 50-60 Hz.

Maximum Rise Time Test, No DUT

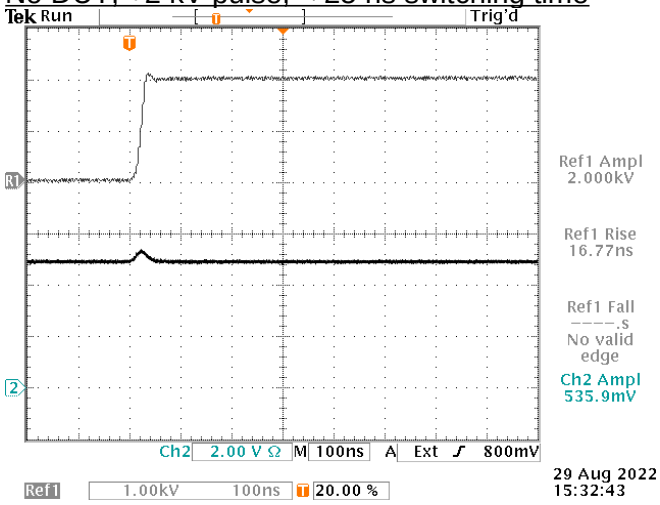


+2 kV, +1.5 kV, -1.5 kV, and -2 kV with maximum rise time setting (1 kV/div, 200 ns/div)

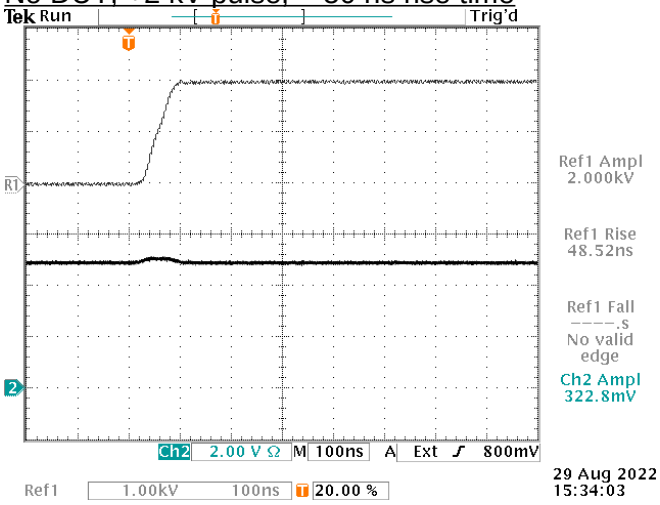


Daughterboard installed
(with no DUT IC)

No DUT, +2 kV pulse, < 25 ns switching time

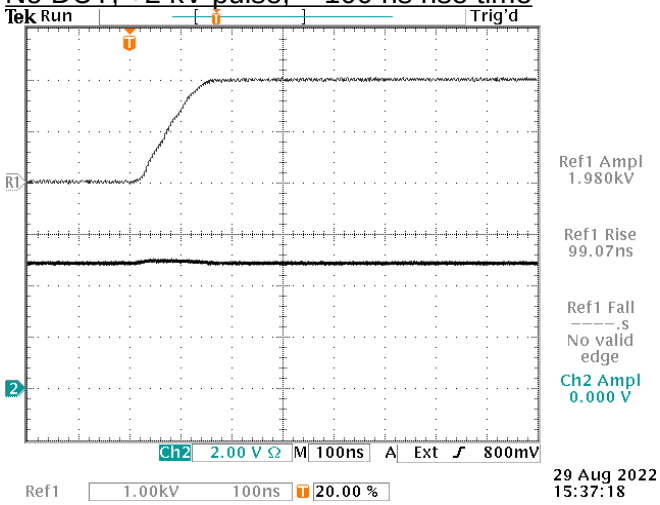


No DUT, +2 kV pulse, ~ 50 ns rise time

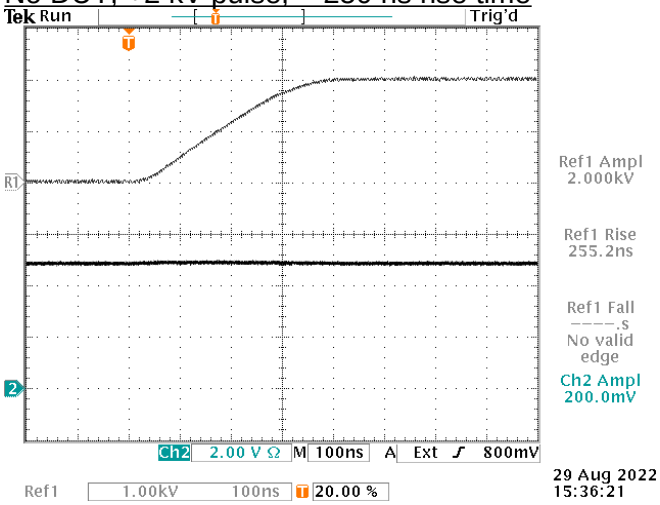


Top = HV out (stored - with signal disconnected before recording logic waveform)
Bottom = Logic out "A" of a standard PCB 267D daughterboard, VCC2 = +5V, using P6246 probe, and no DUT, R2 = 1 kΩ

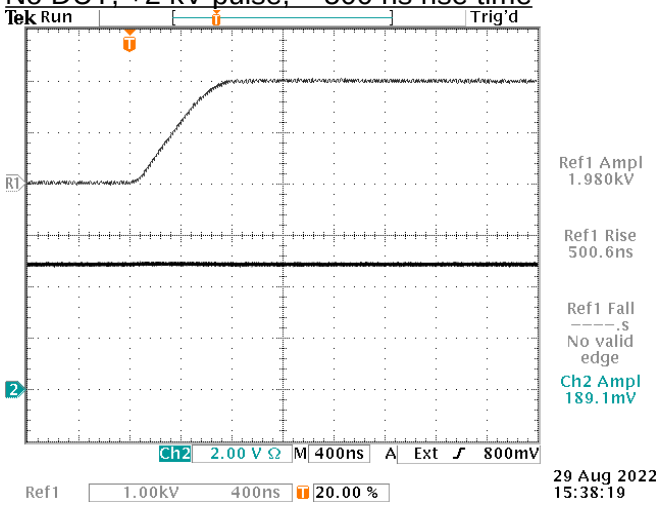
No DUT, +2 kV pulse, ~ 100 ns rise time



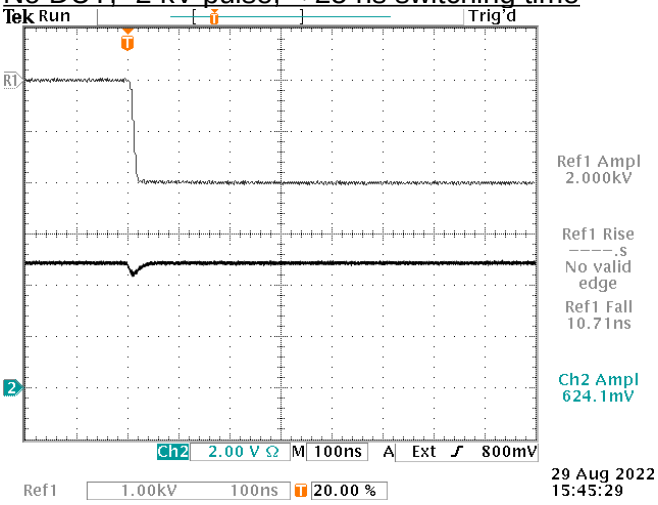
No DUT, +2 kV pulse, ~ 250 ns rise time



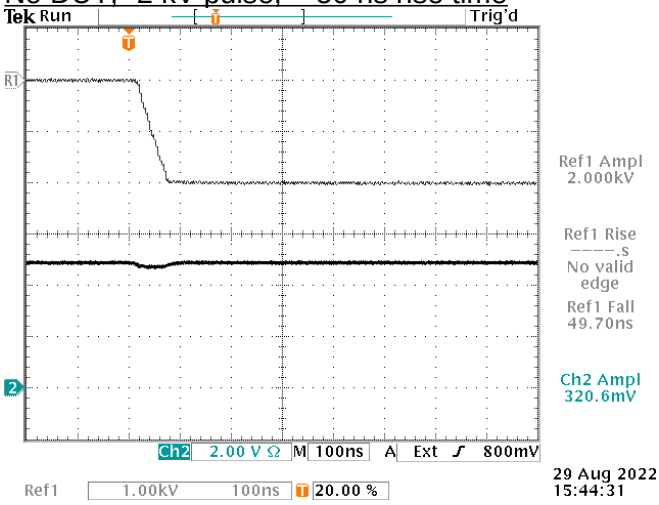
No DUT, +2 kV pulse, ~ 500 ns rise time



No DUT, -2 kV pulse, < 25 ns switching time



No DUT, -2 kV pulse, ~ 50 ns rise time



Top = HV out (stored - with signal disconnected before recording logic waveform)
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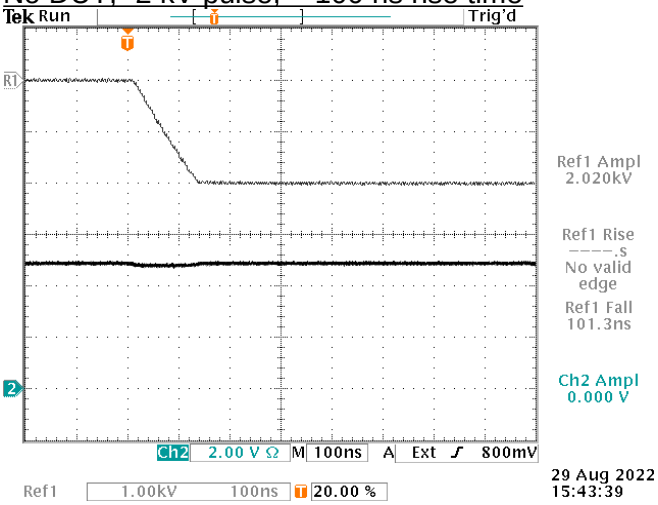
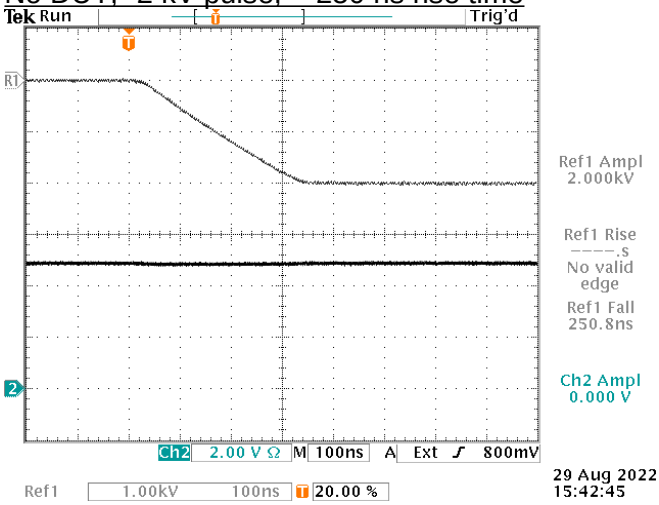
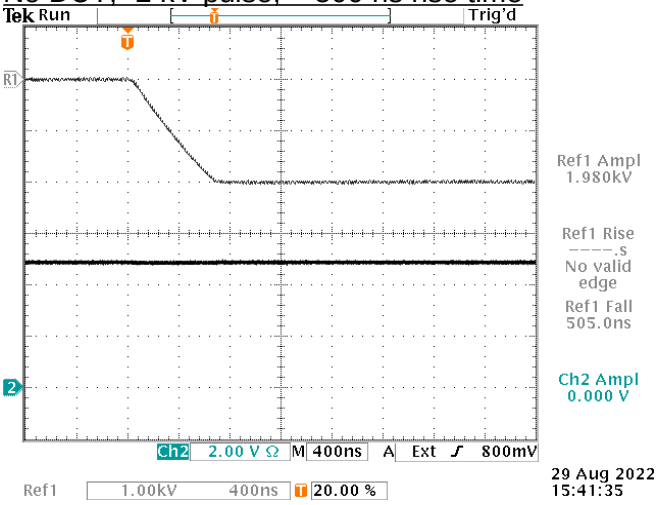
No DUT, -2 kV pulse, ~ 100 ns rise time



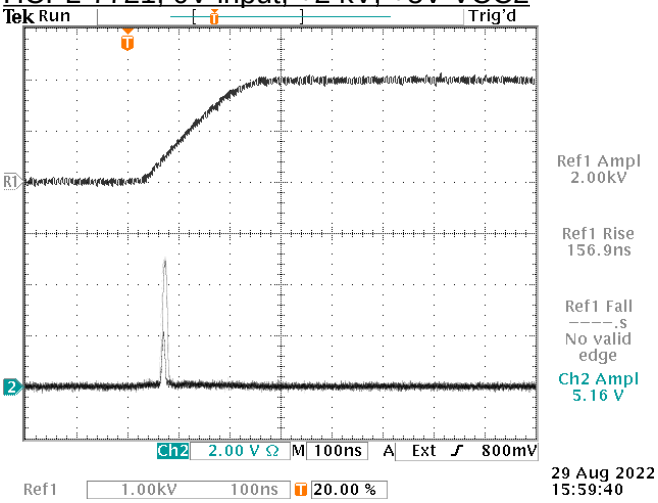
No DUT, -2 kV pulse, ~ 250 ns rise time



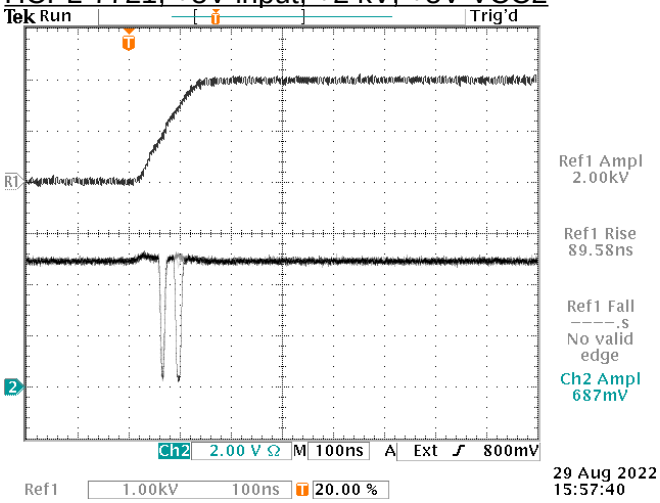
No DUT, -2 kV pulse, ~ 500 ns rise time



HCPL-7721, 0V input, +2 kV, +5V VCC2

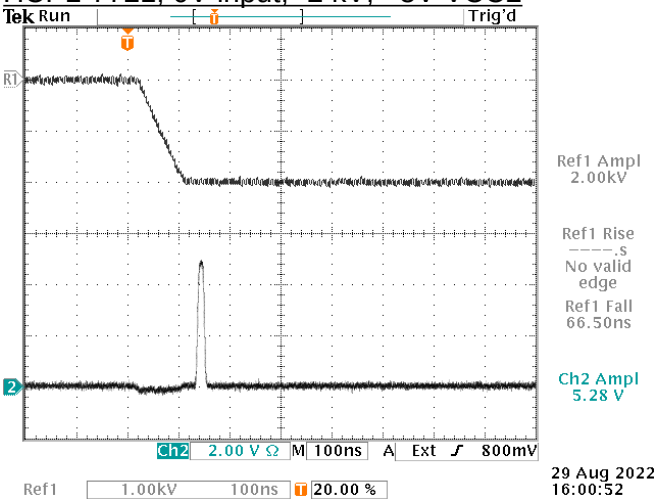


HCPL-7721, +5V input, +2 kV, +5V VCC2

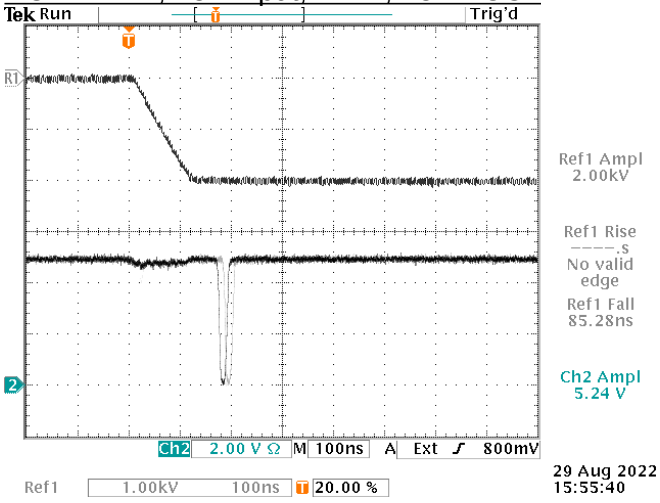


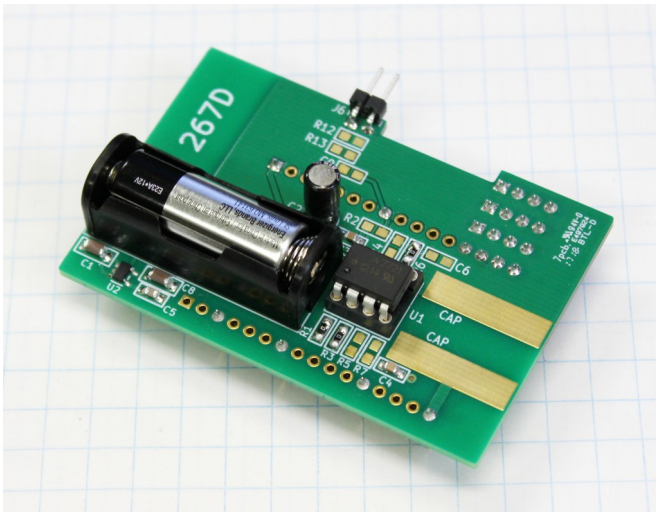
Top = high voltage pulse
Bottom = Logic output

HCPL-7721, 0V input, -2 kV, +5V VCC2

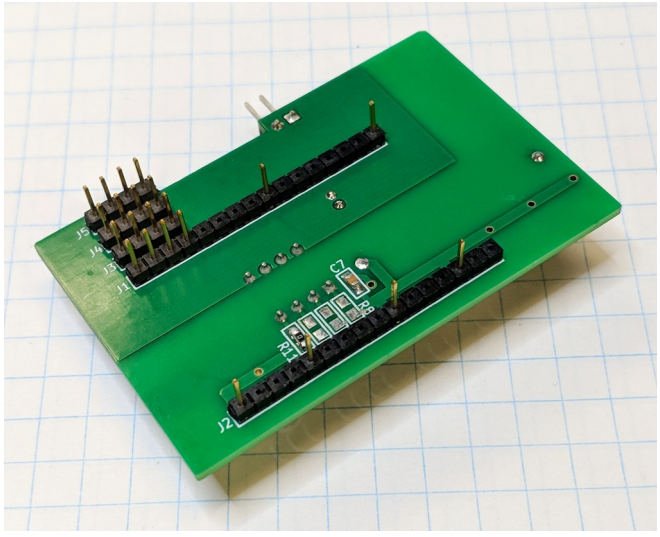


HCPL-7721, +5V input, -2 kV, +5V VCC2





Top side of daughterboard with HCPL-7721 configured for 5V bias.



Bottom side of daughterboard with HCPL-7721 configured for 5V bias.