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BOX 5120, LCD MERIVALE
OTTAWA, CANADA K2C3H5
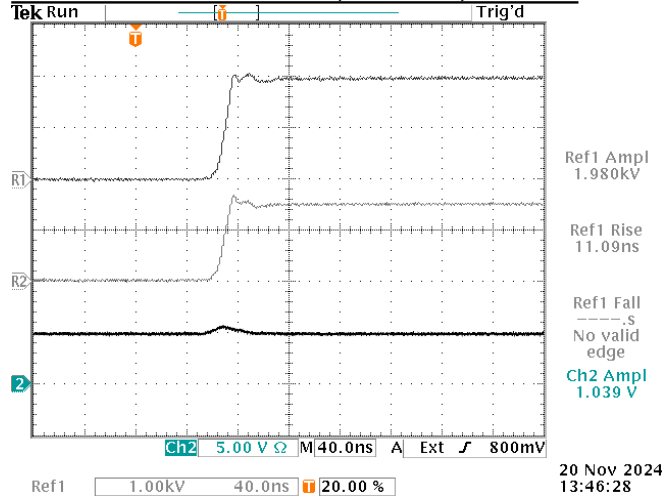
PERFORMANCE CHECKSHEET

Model: AVRQ-5-B-XHV-FPD-AC22-SO16W-ATA3
Type: Common Mode Transient Immunity (CMTI) Test for Opto-Couplers
S.N.:   14487
Date: November 20, 2024

Minimum Rise Time Test, No DUT, Positive

Top = +1.5 and +2.0 kV HV out (stored - with signal disconnected before recording logic waveform).

Bottom = Logic "A" out for +2 kV, VCC2 = +5V, using P6246, and no DUT, R2 = 1 kΩ. (This shows the parasitic capacitive coupling onto the Logic "A" out.)

a) Output Signal Amplitude: ±1.5 to ±2 kV

b) Rise Time (10%-90%): < 15 to > 50 ns

c) PRF: 1 Hz - 100 Hz

d) Jitter, Stability: OK
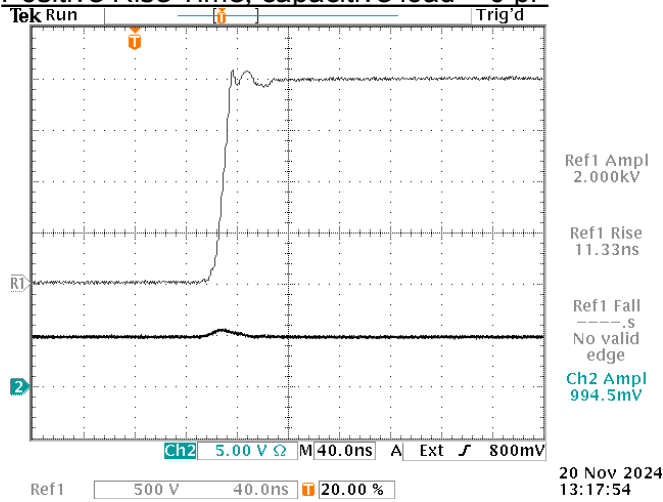
e) Prime Power: 100-240V AC, 50-60 Hz.

Minimum Rise Time Test, No DUT, Negative
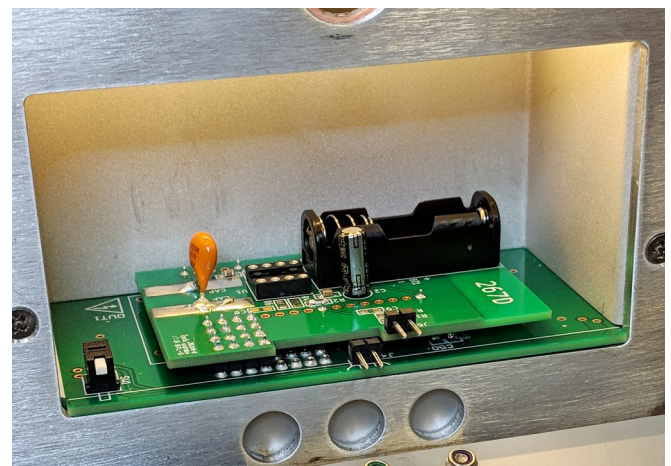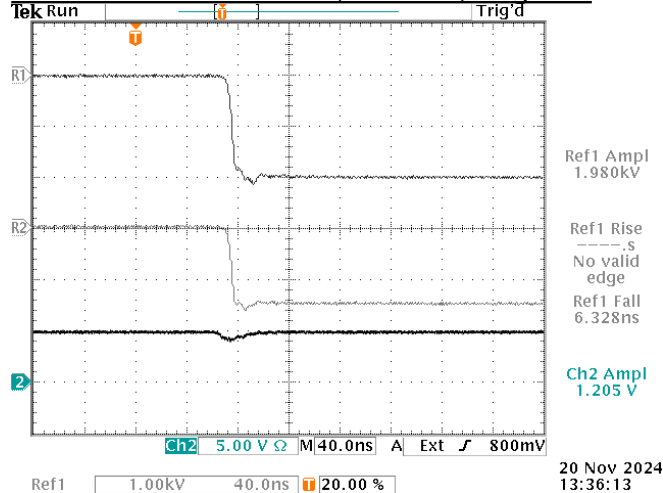
Daughterboard installed
in positive position (with no DUT IC)
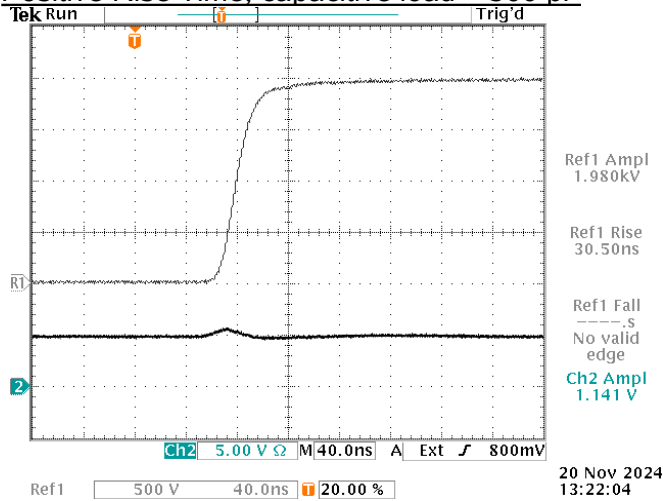
Positive Rise Time, capacitive load = 0 pF
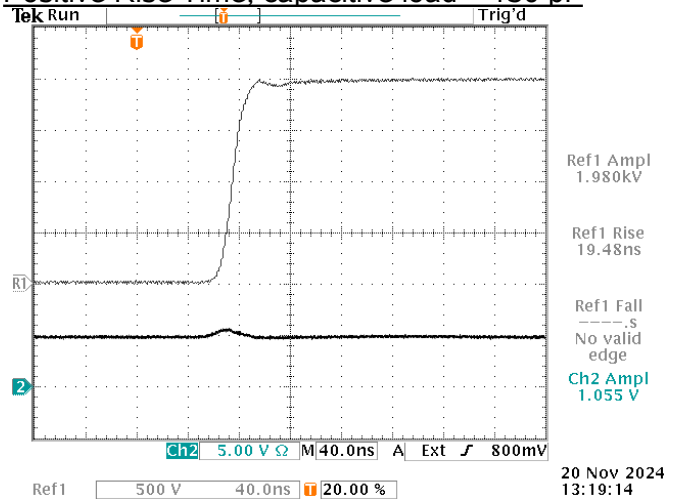
Ref1 Ampl 2.000kV

Ref1 Rise 11.33ns

Ref1 Fall ----.s No valid edge

Ch2 Ampl 994.5mV

Ch2 5.00 V Ω M 40.0ns A Ext ∫ 800mV

Ref1 500 V 40.0ns 20.00 %

20 Nov 2024 13:17:54

Positive Rise Time, capacitive load = 150 pF

Ref1 Ampl 1.980kV

Ref1 Rise 19.48ns

Ref1 Fall ----.s No valid edge

Ch2 Ampl 1.055 V

Ch2 5.00 V Ω M 40.0ns A Ext ∫ 800mV

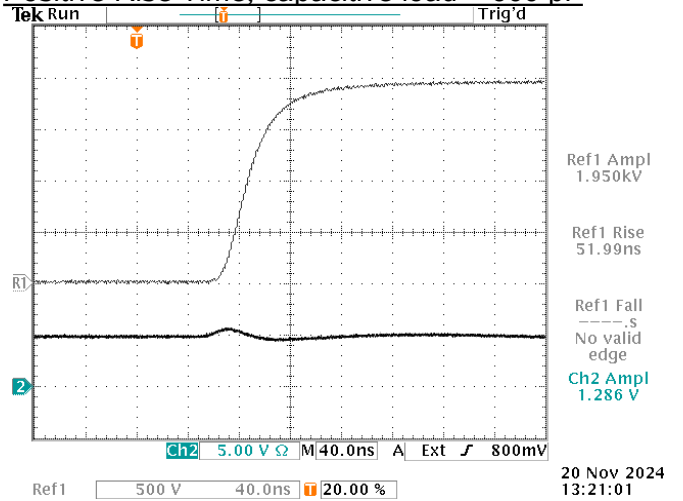Ref1 500 V 40.0ns 20.00 %

20 Nov 2024 13:19:14

Top = HV out (stored - with signal disconnected before recording logic waveform)
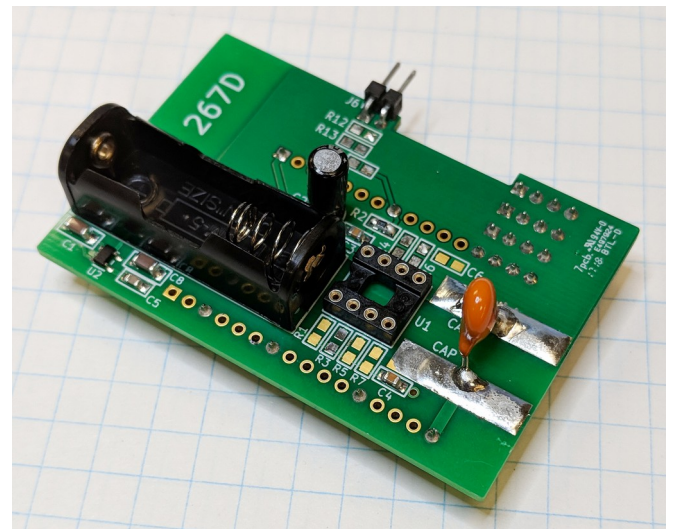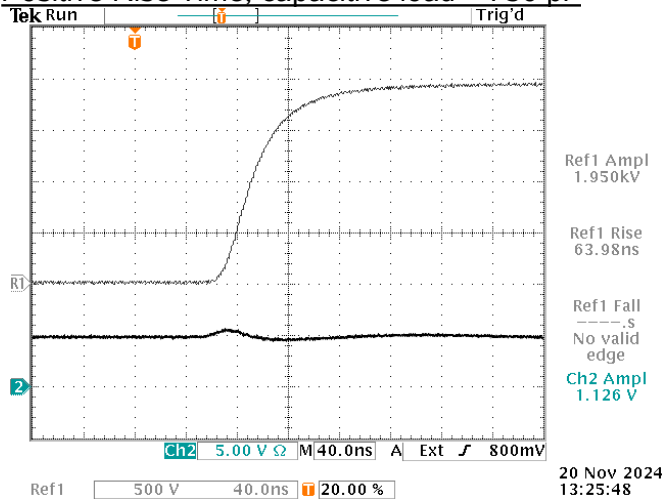Bottom = Logic "A" out, VCC2 = +5V, using P6246 probe, and no DUT, R2 = 1 kΩ

Positive Rise Time, capacitive load = 300 pF

Ref1 Ampl 1.980kV

Ref1 Rise 30.50ns

Ref1 Fall ----.s No valid edge

Ch2 Ampl 1.141 V

Ch2 5.00 V Ω M 40.0ns A Ext ∫ 800mV

Ref1 500 V 40.0ns 20.00 %

20 Nov 2024 13:22:04

Positive Rise Time, capacitive load = 600 pF

Ref1 Ampl 1.950kV

Ref1 Rise 51.99ns

Ref1 Fall ----.s No valid edge

Ch2 Ampl 1.286 V

Ch2 5.00 V Ω M 40.0ns A Ext ∫ 800mV

Ref1 500 V 40.0ns 20.00 %

20 Nov 2024 13:21:01

Positive Rise Time, capacitive load = 750 pF

Ref1 Ampl 1.950kV

Ref1 Rise 63.98ns

Ref1 Fall ----.s No valid edge

Ch2 Ampl 1.126 V

Ch2 5.00 V Ω M 40.0ns A Ext ∫ 800mV

Ref1 500 V 40.0ns 20.00 %

20 Nov 2024 13:25:48

150 pF capacitor (orange) on daughterboard

Negative Rise Time, capacitive load = 0 pF
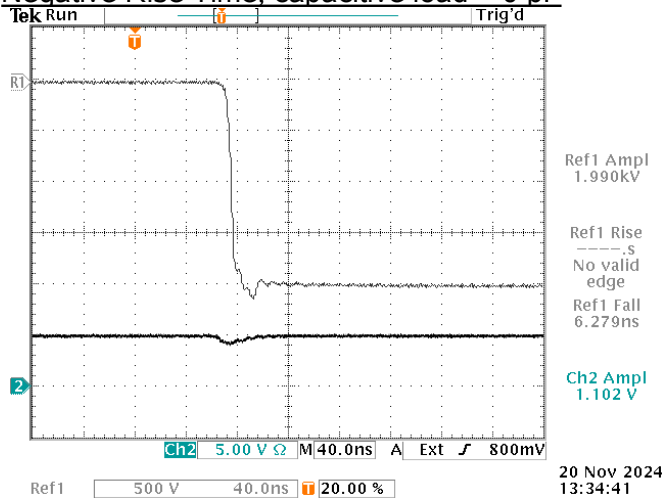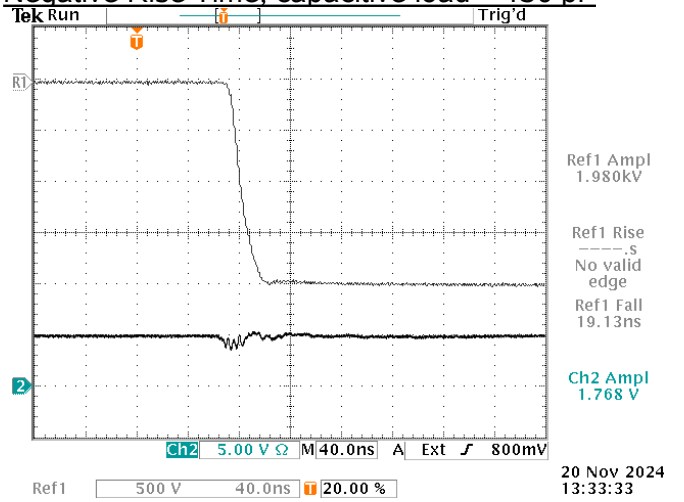
Tek Run   Trig'd

Ref1 Ampl
1.990kV

Ref1 Rise
————.s
No valid
edge

Ref1 Fall
6.279ns

Ch2 Ampl
1.102 V

Ch2   5.00 V Ω   M 40.0ns   A   Ext ∫ 800mV

Ref1   500 V   40.0ns   20.00 %

20 Nov 2024
13:34:41

Negative Rise Time, capacitive load = 150 pF

Tek Run   Trig'd

Ref1 Ampl
1.980kV

Ref1 Rise
————.s
No valid
edge

Ref1 Fall
19.13ns

Ch2 Ampl
1.768 V

Ch2   5.00 V Ω   M 40.0ns   A   Ext ∫ 800mV

Ref1   500 V   40.0ns   20.00 %

20 Nov 2024
13:33:33

Top = HV out (stored - with signal disconnected
before recording logic waveform)
Bottom = Logic "A" out, VCC2 = +5V, using P6246
probe, and no DUT, R2 = 1 kΩ

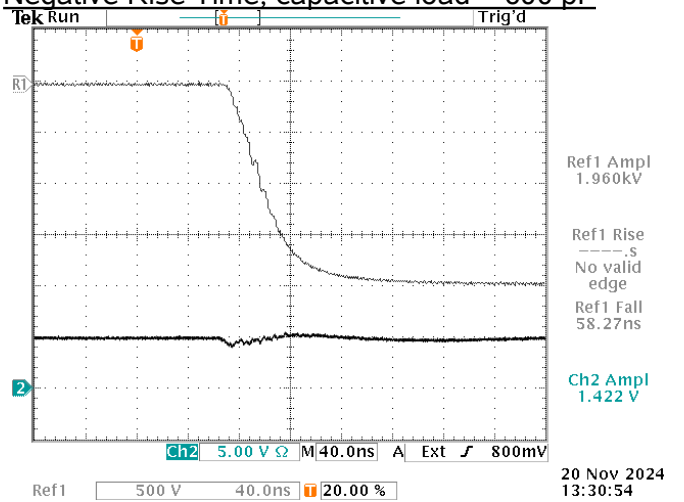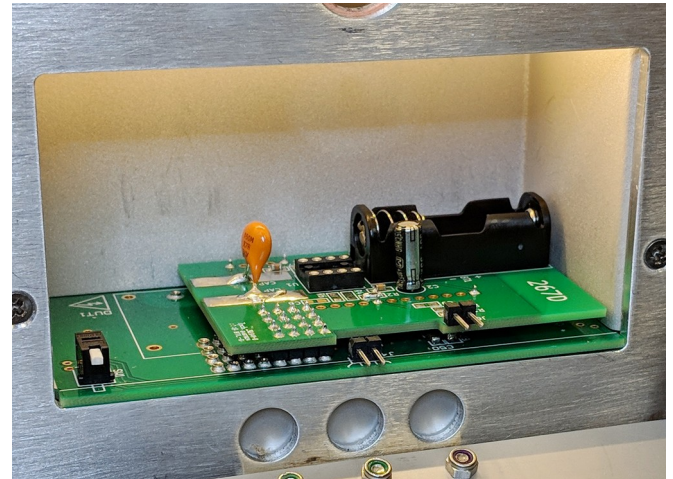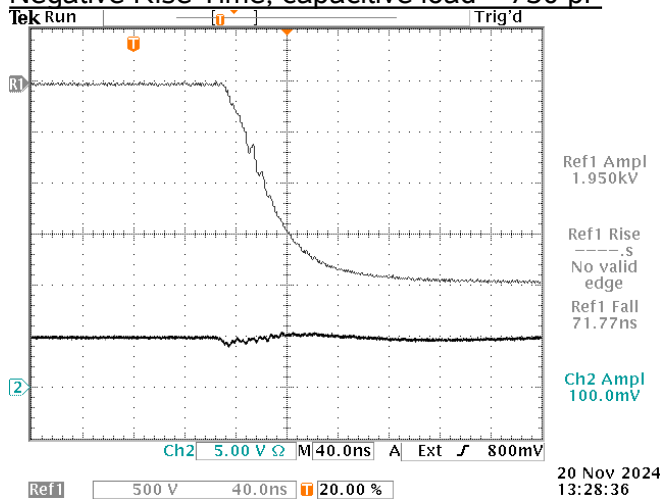## Negative Rise Time, capacitive load = 300 pF
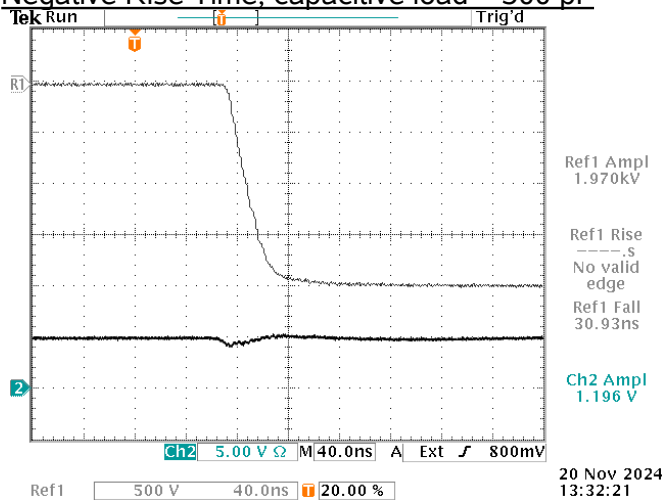
Tek Run   Trig'd

Ref1 Ampl
1.970kV

Ref1 Rise
————.s
No valid
edge

Ref1 Fall
30.93ns

Ch2 Ampl
1.196 V

Ch2   5.00 V Ω   M 40.0ns   A   Ext ∫ 800mV

Ref1   500 V   40.0ns   20.00 %

20 Nov 2024
13:32:21

Negative Rise Time, capacitive load = 600 pF

Tek Run   Trig'd

Ref1 Ampl
1.960kV

Ref1 Rise
————.s
No valid
edge

Ref1 Fall
58.27ns

Ch2 Ampl
1.422 V

Ch2   5.00 V Ω   M 40.0ns   A   Ext ∫ 800mV

Ref1   500 V   40.0ns   20.00 %

20 Nov 2024
13:30:54

Negative Rise Time, capacitive load = 750 pF

Tek Run   Trig'd

Ref1 Ampl
1.950kV

Ref1 Rise
————.s
No valid
edge

Ref1 Fall
71.77ns

Ch2 Ampl
100.0mV

Ch2   5.00 V Ω   M 40.0ns   A   Ext ∫ 800mV

Ref1   500 V   40.0ns   20.00 %

20 Nov 2024
13:28:36

Daughterboard installed
in negative position (with no DUT IC)

HCPL-7721, 0V input, +2 kV, 680 pF added

Ref1 Ampl 1.980kV
Ref1 Rise 27.06ns
Ref1 Fall ----.s No valid edge
Ch2 Ampl 5.728 V

Ch2 5.00 V Ω M 40.0ns A Ext ʃ 800mV
Ref1 1.00kV 40.0ns 20.00 %

20 Nov 2024 13:58:53

HCPL-7721, 5V input, +2 kV, 680 pF added

Ref1 Ampl 1.960kV
Ref1 Rise 31.15ns
Ref1 Fall ----.s No valid edge
Ch2 Ampl 6.075 V

Ch2 5.00 V Ω M 40.0ns A Ext ʃ 800mV
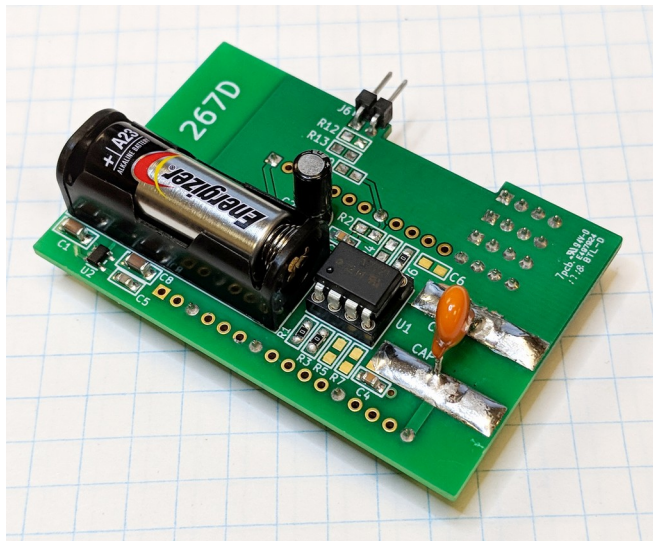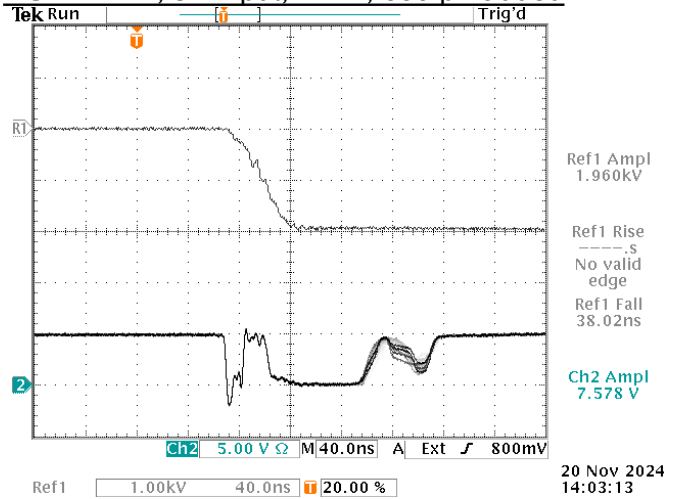Ref1 1.00kV 40.0ns 20.00 %

20 Nov 2024 14:04:23
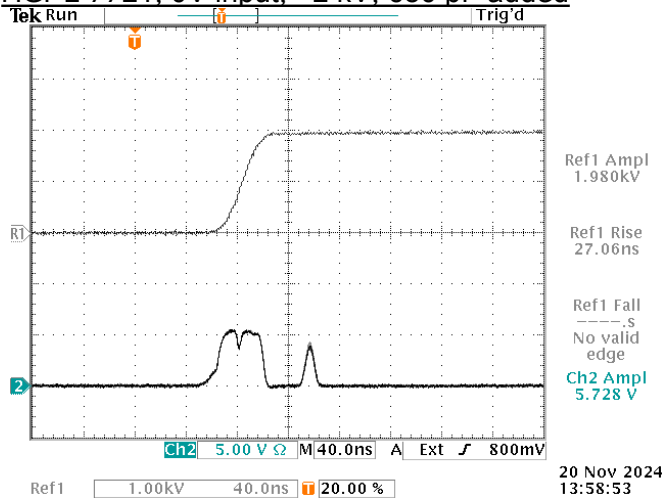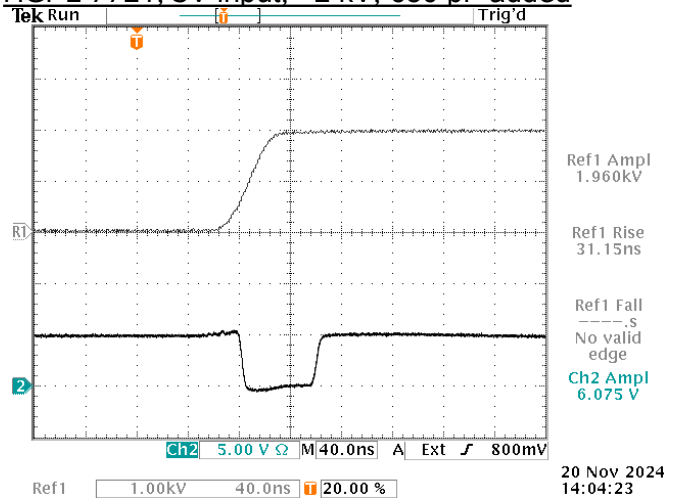
Top = high voltage pulse (stored - with signal disconnected before recording logic waveform).
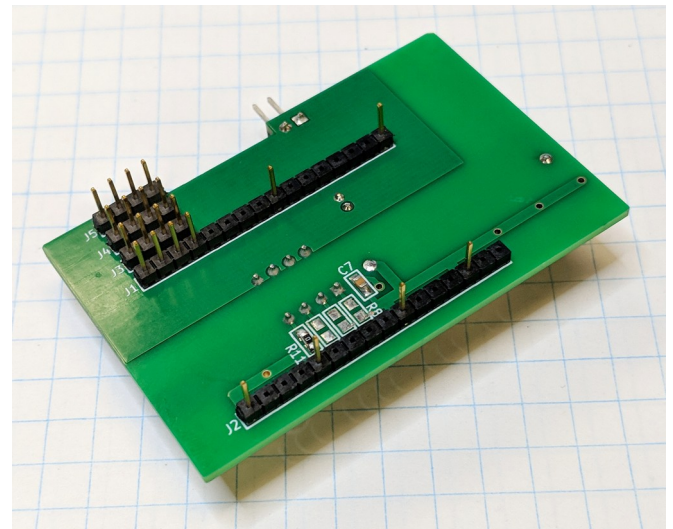
Bot = Logic "A" out (with 0V input) using P6246.

HCPL-7721, 0V input, -2 kV, 680 pF added

Ref1 Ampl 1.960kV
Ref1 Rise ----.s No valid edge
Ref1 Fall 35.84ns
Ch2 Ampl 4.800 V

Ch2 5.00 V Ω M 40.0ns A Ext ʃ 800mV
Ref1 1.00kV 40.0ns 20.00 %

20 Nov 2024 14:00:56

HCPL-7721, 5V input, -2 kV, 680 pF added

Ref1 Ampl 1.960kV
Ref1 Rise ----.s No valid edge
Ref1 Fall 38.02ns
Ch2 Ampl 7.578 V

Ch2 5.00 V Ω M 40.0ns A Ext ʃ 800mV
Ref1 1.00kV 40.0ns 20.00 %

20 Nov 2024 14:03:13
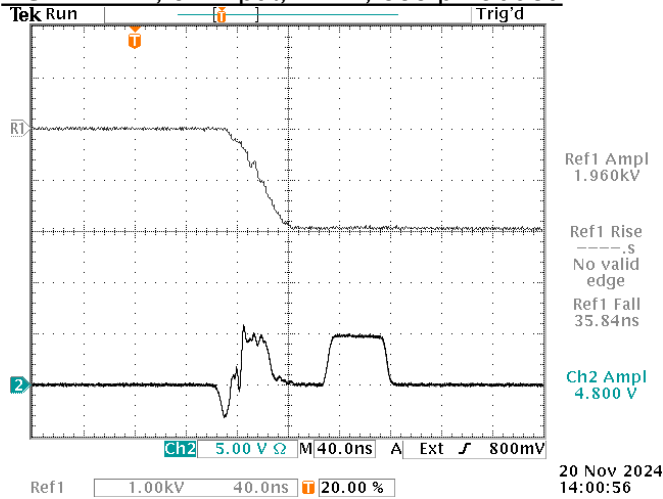
Top side of daughterboard with HCPL-7721 configured for 5V bias.

Bottom side of daughterboard with HCPL-7721 configured for 5V bias.

/fileserver1/production/check-sheets/sn14xxx/sn14487,AVRQ-5-B-XHV-FPD-AC22-SO16W-ATA3.odt