AVTECH ELECTROSYSTEMS LTD.

NANOSECOND WAVEFORM ELECTRONICS
SINCE 1975

P.O. BOX 265
OGDENSBURG, NY
U.S.A. 13669-0265

TEL: 888-670-8729 (USA & Canada) or +1-613-686-6675 (Intl)
FAX: 800-561-1970 (USA & Canada) or +1-613-686-6679 (Intl)

info@avtechpulse.com - http://www.avtechpulse.com/

BOX 5120, LCD MERIVALE
OTTAWA, ONTARIO
CANADA K2C 3H5

INSTRUCTIONS

MODEL AVR-EBF6-B

UP TO +1 Amp

FORWARD RECOVERY

t_{FR} / V_{FR} MEASUREMENT SYSTEM

SERIAL NUMBER: _____

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

TECHNICAL SUPPORT

Phone: 888-670-8729 (USA & Canada) or +1-613-686-6675 (Intl)
Fax: 800-561-1970 (USA & Canada) or +1-613-686-6679 (Intl)

E-mail: info@avtechpulse.com
World Wide Web: http://www.avtechpulse.com

TABLE OF CONTENTS

Manual Reference: /fileserver1/officefiles/instructword/avr-eb/avr-ebf6-b/AVR-EBF6-B,ed9.odt.
Last modified February 29, 2024.

INTRODUCTION

The AVR-EBF6-B is a high performance, GPIB and RS232-equipped test system for measuring the t_{FR} and V_{FR} forward recovery characteristics of high speed rectifiers.

The AVR-EBF6-B consists of three main components:

1. The instrument mainframe, which generates voltage pulses in the range of +2.5 (or +0.5V for units with the -FTA option) to +50V with rise times < 5 ns.

2. A rise time filter, which increases the rise time of the voltage pulse to 10 ns (or optionally 8 ns, 12 ns, or 20 ns), ±20%.

3. A test jig, into which the device under test (DUT) is inserted.

Depending on the options and accessories ordered, the instrument may be supplied with more than one rise time filter and more than one test jig.

The mainframe connects to the rise time filter using a length of coaxial cable. The output of the filter connects to the test jig using another length of coaxial cable. A control cable connects the mainframe to the test jig, to control the safety interlocks. The two test jig outputs are fed into the 50 Ohm inputs of an oscilloscope by two lengths of coaxial cable.

The (user-supplied) oscilloscope is used to measure the V_{FR} and t_{FR} values based on the waveforms from the test jig outputs.

The waveforms generated by this instrument are suitable for MIL-STD-750E Method 4026.3 tests. In the terminology of this standard:

- I_F = 50 mA (10 mA for units with the -FTA option) up to 1 A
- Rise Time = 10 ns (unless the optional 8, 12, or 20 ns filters are used)
- Pulse width t1 = 200 ns to 10 us (200 ns to 500 ns for -DIPFP models)
- Generator Resistance R_S = 50 Ohms
- Pulse frequency = 1 Hz to 100 Hz
- Response detector input impedance Z = 500 Ohms

The test jig supplied with the instrument is carefully constructed such that the parasitic inductance is minimized. This prevents overestimation of V_{FR}, and provides increased t_{FR} accuracy.

Standard AVR-EBF6-B models include one AVX-TFR-MIX diode test jig. This standard test jig contains a variety of pin sockets and posts, which may be used to hold the diode device under test (DUT). The test jig has a hinged lid, which must be fully closed to protect the user from high voltages. The output will be automatically disabled if the lid is left open. The standard AVR-TFR-MIX test jig will accommodate TO-220AC (2 lead)

packages, DO-style packages with leads bent at 90°, and standard and reverse-polarity TO-3 packages.

This instrument may be ordered with the AVX-TFR-ANB test jig instead (-ANB option). This test jig accepts DO-41 and Microsemi Type E packages. In contrast to the AVX-TFR-MIX, no lead bending is required.

This instrument may also be ordered with the AVX-TRR-DIPFP test jig instead (-DIPFP option). This test jig accepts DIP packages with 0.3” row spacing, with up to 16 pins. A plug-in DIP-to-flat-pack adapter is also provided, to permit testing of military-style flat-packs, again with up to 16 pins. The test jig contains a series of relays, permit the input and output signals to be switched to any of the 16 pins. The pins may be set from the front panel or by computer command.

Test jigs accommodating MELF packages (AVX-TFR-MELF) and DO-4 and DO-5 stud packages (AVX-TFR-STUD) can also be provided as separate accessories.

While the provided test jig is intended to be flexible and easy to use, users can also develop their own test jigs easily.

The AVR-EBF6-B includes an internal trigger source, but it can also be triggered or gated by an external source. A front-panel pushbutton can also be used to trigger the instrument.

The AVR-EBF6-B features front panel keyboard and adjust knob control of the output pulse parameters along with a four line by 40-character backlit LCD display of the output amplitude, pulse repetition frequency, and delay. The instrument includes memory to store up to four complete instrument setups. The operator may use the front panel or the computer interface to store a complete “snapshot” of all key instrument settings, and recall this setup at a later time.

This instrument is intended for use in research, development, test and calibration laboratories by qualified personnel.

SPECIFICATIONS

Model[1]:	AVR-EBF6-B
Recovery type:	Forward recovery
Intended application:	High-speed rectifiers
Basic waveform:	A positive pulse
Pulse polarity:	+
Voltage output[2,5,7]: (to R_L = 50Ω)	+2.5V to +50V (standard models) +0.5V to +50V (with -FTA option)
Corresponding diode current[2,5] (approx., depends on V_{DIODE}):	+50 mA to +1A (standard models) +10 mA to +1A (with -FTA option)
Pulse width (FWHM):	200 ns to 10 us[8]
Rise time (10%-90%):	No filter < 5 ns. Standard filter[4]: 10 ns Optional filters[4]: 8 ns, 12 ns, 20 ns
Output impedance during pulse (inside the mainframe):	50 Ohms
Maximum PRF:	100 Hz
Delay:	0 to ±1s, variable
Included test jig[3]:	See table on next page.
GPIB & RS-232:	Standard on -B units. See http://www.avtechpulse.com/gpib for details.
Ethernet port, for remote control using VXI-11.3, ssh, telnet, & web:	Optional[12]. Recommended as a modern alternative to GPIB / RS-232. See http://www.avtechpulse.com/options/vxi for details.
Settings resolution:	The resolution of the timing parameters varies, but is always better than 0.15% of the set value. The amplitude and offset resolution is typically 0.02% of the maximum amplitude.
Settings accuracy:	Typically ± 3% after 10 minute warmup, for timing parameter. For high-accuracy applications requiring traceable calibration, verify the output parameters with a calibrated oscilloscope[5].
Trigger required:	External trigger mode: + 5 Volts, 10 ns or wider (TTL)
Gate input:	Active high or low, switchable. Suppresses triggering when active.
Power requirements:	100 - 240 Volts, 50 - 60 Hz
Dimensions:	H x W x D: 100 mm x 430 mm x 375 mm (3.9" x 17" x 14.8")
Chassis material:	cast aluminum frame and handles, blue vinyl on aluminum cover plates
Temperature range:	+5°C to +40°C

1) -B suffix indicates IEEE-488.2 GPIB and RS-232 control of amplitude, pulse width, PRF and delay (see http://www.avtechpulse.com/gpib).
2) For operation at amplitudes of less than 10% of full-scale, best results will be obtained by setting the amplitude near full-scale and using external attenuators on the output.
3) Customized jigs available upon request.
4) The 10 ns (10%-90%) rise time filter is included as a standard feature. To add an 8 ns filter, add the -F8NS option to the model number. To add a 12 ns filter, add the -F12NS option to the model number. To add a 20 ns filter, add the -F20NS option to the model number. The rise time filter rise time accuracy is ±20%.
5) The amplitude settings should not be relied upon for any degree of accuracy, because the dynamics of the device under test can affect the actual generated waveforms. Amplitude settings should always be verified by oscilloscope measurements.
6) Thus the diode must come to forward steady-state within 500 ns.
7) The diode must have a breakdown voltage exceeding these amplitude limits. Contact Avtech for special arrangements if $I_{MAX} \times 50\Omega > V_{BR}$.
8) Maximum pulse width is reduced to 500 ns for units with the -DIPFP option.
9) The full forward pulse width is 2 us, but the reverse pulse is super-imposed on the forward pulse 500 ns after the start of the forward pulse.
10) Increases to 4.5 ns for units with the -DIPFP option, due to the switching relay inductance.
11) Depends on the parasitic inductance of the DUT and its leads.
12) Add the suffix -VXI to the model number to specify the Ethernet port.

SPECIFICATIONS – INCLUDED TEST JIGS

Option Code	Included Jig	Description
standard	AVX-TFR-MIX	Includes a mix of pin sockets. Will accept TO-220AC (2 lead) packages, DO-style packages[3] (DO-15, DO-35, DO-41, DO-201AD, etc.) with leads bent at 90°, and standard and reverse-polarity TO-3 packages. Lead bending is required for axial packages.
-ANB	AVX-TFR-ANB	"Axial no bend" jig. Accepts will accept DO-41 packages (0.205" x 0.107" body, max) and Microsemi Axial Type E packages (0.185" x 0.135" body, max). Unlike the standard jig, bending is NOT required to insert these packages. This jig will not accept any other type of package.
-MELF	AVX-TRR-MELF	MELF jig. Accepts most common MELF and SQMELF packages. Uses two opposing spring pins, which much be pulled back using tweezers while maneuvering the DUT into position.
-SQMELF	AVX-TFR-SQMELF	Square MELF jig. Accepts Microsemi Type A (D-5A) and Microsemi Type E (D-5B) "square MELF" packages. It also accepts Microsemi Type B (D-5D) and Microsemi Type G (D-5C) packages, although the fit is less optimal. Easier to use (tweezers are not required to open the device holder), but less flexible, than the -MELF option.
-DIPFP	AVX-TFR-DIPFP	DIP / flat-pack jig. Accepts DIP packages with up to 16 pins (width = 0.3", pitch = 0.1"). A flat-pack-to-DIP adapter is provided to accept mil-style flat-packs with up to 16 pins (width < 0.27", pitch = 0.050"). The instrument can be programmed to switch the input and output signals to any pair of pins on the device under test, using a system of internal relays. This is not available as a separate part number. It must be ordered as an option when ordering the AVR-EB-series instrument.
-AR1	AVX-TFR-AR1	Axial / square MELF jig with customized Aries 9890-122-23 socket. Accepts: 1. Microsemi "Type E" axial packages (used in the 1N5418 and other devices) 2. Generic DO-41 packages (used in the 1N5819 and other devices) 3. Microsemi Type A square MELF, also called D-5A (for example, 1N5806US) 4. Microsemi Type B square MELF, also called D-5D (for example, 1N6701US) 5. Microsemi Type E square MELF, also called D-5B (for example, 1N5811US)
-STUD	AVX-TFR-STUD	Stud jig. Accepts DO-4 and DO-5 stud packages.

NOTE: *All of the above jigs are suitable for light research and development use. Consult Avtech (info@avtechpulse.com) regarding the suitability of particular jigs for heavy production use.*

REGULATORY NOTES

FCC PART 18

This device complies with part 18 of the FCC rules for non-consumer industrial, scientific and medical (ISM) equipment.

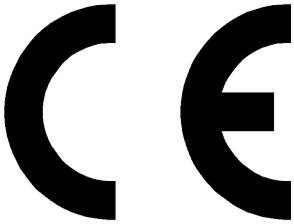
This instrument is enclosed in a rugged metal chassis and uses a filtered power entry module (where applicable). The main output signal is provided on a shielded connector that is intended to be used with shielded coaxial cabling and a shielded load. Under these conditions, the interference potential of this instrument is low.

If interference is observed, check that appropriate well-shielded cabling is used on the output connectors. Contact Avtech (info@avtechpulse.com) for advice if you are unsure of the most appropriate cabling. Also, check that your load is adequately shielded. It may be necessary to enclose the load in a metal enclosure.

If any of the connectors on the instrument are unused, they should be covered with shielded metal “dust caps” to reduce the interference potential.

This instrument does not normally require regular maintenance to minimize interference potential. However, if loose hardware or connectors are noted, they should be tightened. Contact Avtech (info@avtechpulse.com) if you require assistance.

EC DECLARATION OF CONFORMITY



We Avtech Electrosystems Ltd.
P.O. Box 5120, LCD Merivale
Ottawa, Ontario
Canada K2C 3H5

declare that this pulse generator meets the intent of Directive 2004/108/EG for Electromagnetic Compatibility. Compliance pertains to the following specifications as listed in the official Journal of the European Communities:

EN 50081-1 Emission

EN 50082-1 Immunity

and that this pulse generator meets the intent of the Low Voltage Directive 72/23/EEC as amended by 93/68/EEC. Compliance pertains to the following specifications as listed in the official Journal of the European Communities:

EN 61010-1:2001	Safety requirements for electrical equipment for measurement, control, and laboratory use

DIRECTIVE 2002/95/EC (RoHS)

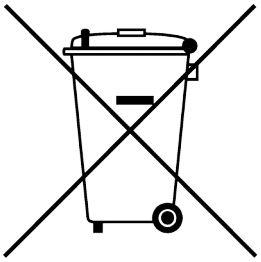
This instrument is exempt from Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment. Specifically, Avtech instruments are considered "Monitoring and control instruments" (Category 9) as defined in Annex 1A of Directive 2002/96/EC. The Directive 2002/95/EC only applies to Directive 2002/96/EC categories 1-7 and 10, as stated in the "Article 2 - Scope" section of Directive 2002/95/EC.

DIRECTIVE 2002/96/EC (WEEE)

European customers who have purchased this equipment directly from Avtech will have completed a “WEEE Responsibility Agreement” form, accepting responsibility for WEEE compliance (as mandated in Directive 2002/96/EC of the European Union and local laws) on behalf of the customer, as provided for under Article 9 of Directive 2002/96/EC.

Customers who have purchased Avtech equipment through local representatives should consult with the representative to determine who has responsibility for WEEE compliance. Normally, such responsibilities with lie with the representative, unless other arrangements (under Article 9) have been made.

Requirements for WEEE compliance may include registration of products with local governments, reporting of recycling activities to local governments, and financing of recycling activities.



AC POWER SUPPLY REGULATORY NOTES

This instrument converts the AC input power to the +24V DC voltage that powers the internal circuitry of this instrument using a Tamura AAD130SD-60-A switching power supply. According to the manufacturer, the Tamura AAD130SD-60-A has the following certifications:

UL60950-1
IEC60950 -1
CSA C22.2 No. 60950- 1
EN60950 -1

and is compliant with:

EN61000-3-2
EN61000-4-2 Level 2
EN61000-4-2 Level 3 (Air Only)
EN61000-4-4 Level 3
EN61000-4-5 Level 3
EN61000-4-11
CISPR 11 and 22 FCC Part 15 Class B (conducted)

FIRMWARE LICENSING

Instruments with firmware versions 5.00 or higher use open-source software internally. Some of this software requires that the source code be made available to the user as a condition of its licensing. This source code is available upon request (contact info@avtechpulse.com).

Earlier firmware versions do not contain any open source software.

INSTALLATION

VISUAL CHECK

After unpacking the instrument, examine to ensure that it has not been damaged in shipment. Visually inspect all connectors, knobs, liquid crystal displays (LCDs), and the handles. If the instrument has been damaged, file a claim immediately with the company that transported the instrument.

The following items should be with the instrument:

1) A power cord.
2) A GPIB cable.
3) Two instrumentation manuals (this manual and the “Programming Manual for -B Instruments”).
4) One test jig, with a hinged lid. Units with the -DIPFP option will also have a removable DIP-to-flat-pack adapter installed inside the test jig, and a DIP extractor tool.
5) A 2 meter DB-9 or DB-25 control cable.
6) Two 60 cm lengths of SMA-to-BNC cable.
7) Two 60 cm lengths of SMA-to-SMA cable.
8) One AVX-FILT-10NS accessory filter.
9) Units with -F8NS option only: One AVX-FILT-8NS accessory filter.
10) Units with -F12NS option only: One AVX-FILT-12NS accessory filter.
11) Units with -F20NS option only: One AVX-FILT-20NS accessory filter.

POWER RATINGS

This instrument is intended to operate from 100 - 240 V, 50 - 60 Hz.

The maximum power consumption is 57 Watts. Please see the “FUSES” section for information about the appropriate AC and DC fuses.

This instrument is an “Installation Category II” instrument, intended for operation from a normal single-phase supply.

CONNECTION TO THE POWER SUPPLY

An IEC-320 three-pronged recessed male socket is provided on the back panel for AC power connection to the instrument. One end of the detachable power cord that is supplied with the instrument plugs into this socket. The other end of the detachable power cord plugs into the local mains supply. Use only the cable supplied with the instrument. The mains supply must be earthed, and the cord used to connect the instrument to the mains supply must provide an earth connection. (The supplied cord does this.)

⚠ Warning: Failure to use a grounded outlet may result in injury or death due to electric shock. This product uses a power cord with a ground connection. It must be connected to a properly grounded outlet. The instrument chassis is connected to the ground wire in the power cord.

The table below describes the power cord that is normally supplied with this instrument, depending on the destination region:

Destination Region	Description	Option	Manufacturer	Part Number
United Kingdom, Hong Kong, Singapore, Malaysia	BS 1363, 230V, 50 Hz	-AC00	Qualtek	370001-E01
Australia, New Zealand	AS 3112:2000, 230-240V, 50 Hz	-AC01	Qualtek	374003-A01
Continental Europe, Korea, Indonesia, Russia	European CEE 7/7 “Schuko” 230V, 50 Hz	-AC02	Qualtek	364002-D01
North America, Taiwan	NEMA 5-15, 120V, 60 Hz	-AC03	Qualtek	312007-01
Switzerland	SEV 1011, 230V, 50 Hz	-AC06	Qualtek	378001-E01
South Africa, India	SABS 164-1, 220-250V, 50 Hz	-AC17	Volex	2131H 10 C3
Japan	JIS 8303, 100V, 50-60 Hz	-AC18	Qualtek	397002-01
Israel	SI 32, 220V, 50 Hz	-AC19	Qualtek	398001-01
China	GB 1002-1, 220V, 50 Hz	-AC22	Volex	2137H 10 C3

PROTECTION FROM ELECTRIC SHOCK

⚠ Operators of this instrument must be protected from electric shock at all times. The owner must ensure that operators are prevented access and/or are insulated from every connection point. In some cases, connections must be exposed to potential human contact. Operators must be trained to protect themselves from the risk of electric shock. This instrument is intended for use by qualified personnel who recognize shock hazards and are familiar with safety precautions required to avoid possibly injury. In particular, operators should:

1. Keep exposed high-voltage wiring to an absolute minimum.

2. Wherever possible, use shielded connectors and cabling.

3. Connect and disconnect loads and cables only when the instrument is turned off.

4. Keep in mind that all cables, connectors, oscilloscope probes, and loads must have an appropriate voltage rating.

5. Do not attempt any repairs on the instrument, beyond the fuse replacement procedures described in this manual. Contact Avtech technical support (see page 2 for contact information) if the instrument requires servicing. Service is to be performed solely by qualified service personnel.

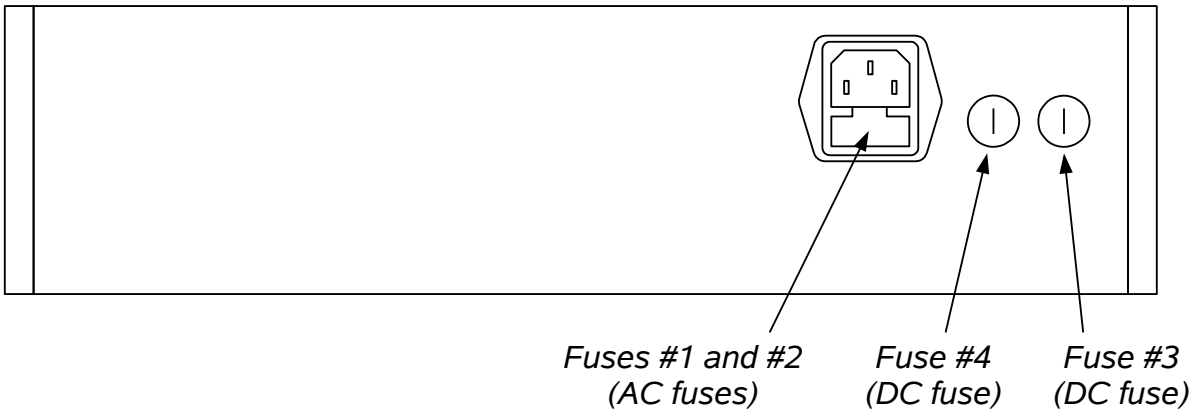
ENVIRONMENTAL CONDITIONS

This instrument is intended for use under the following conditions:

1. indoor use;
2. altitude up to 2 000 m;
3. temperature 5 °C to 40 °C;
4. maximum relative humidity 80 % for temperatures up to 31 °C decreasing linearly to 50 % relative humidity at 40 °C;
5. Mains supply voltage fluctuations up to ±10 % of the nominal voltage;
6. no pollution or only dry, non-conductive pollution.

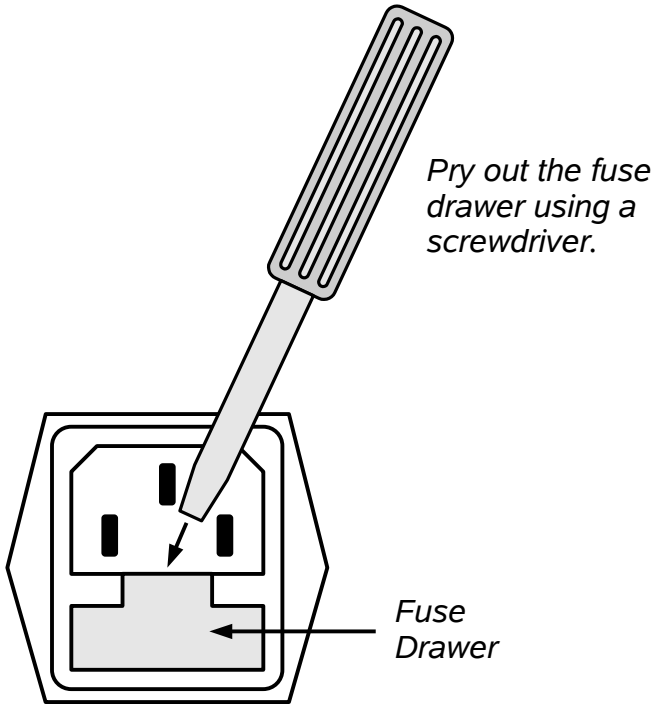
FUSES

This instrument contains four fuses. All are accessible from the rear-panel. Two protect the AC prime power input, and two protect the internal DC power supplies. The locations of the fuses on the rear panel are shown in the figure below:



AC FUSE REPLACEMENT

To physically access the AC fuses, the power cord must be detached from the rear panel of the instrument. The fuse drawer may then be extracted using a small flat-head screwdriver, as shown below:



DC FUSE REPLACEMENT

The DC fuses may be replaced by inserting the tip of a flat-head screwdriver into the fuse holder slot, and rotating the slot counter-clockwise. The fuse and its carrier will then pop out.

FUSE RATINGS

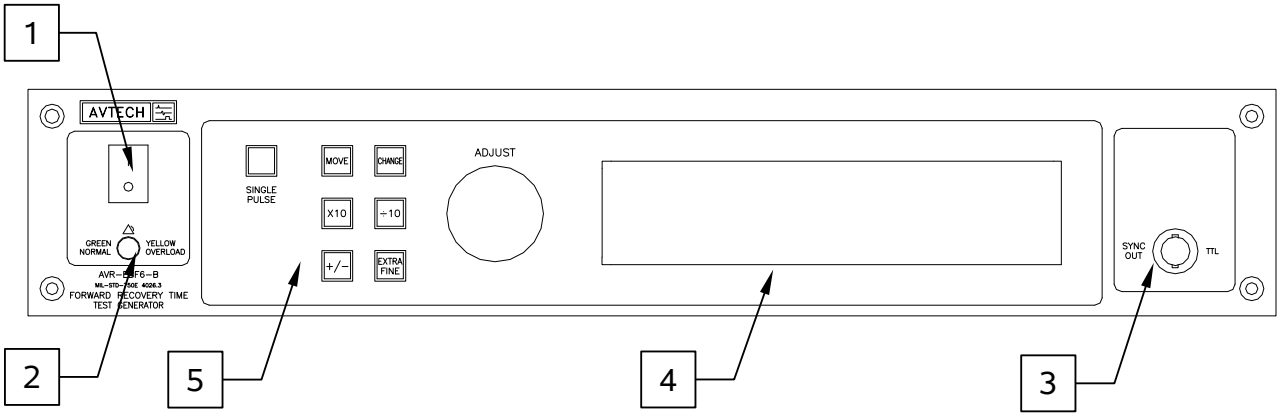
The following table lists the required fuses:

Fuses	Nominal Mains Voltage	Rating	Case Size	Recommended Replacement Part	
				Littelfuse Part Number	Digi-Key Stock Number
#1, #2 (AC)	100-240V	0.5A, 250V, Time-Delay	5×20 mm	0218.500HXP	F2416-ND
#3 (DC)	N/A	1.6A, 250V, Time-Delay	5×20 mm	021801.6HXP	F2424-ND
#4 (DC)	N/A	0.5A, 250V, Time-Delay	5×20 mm	0218.500HXP	F2416-ND

The recommended fuse manufacturer is Littelfuse (http://www.littelfuse.com).

Replacement fuses may be easily obtained from Digi-Key (http://www.digikey.com) and other distributors.

FRONT PANEL CONTROLS



1. POWER Switch. This is the main power switch. When turning the instrument on, there is normally a delay of 5-10 seconds before anything is shown on the main display.

   If the main menu does not appear after 30 seconds, turn off the instrument and leave it off for at least 60 seconds before applying power again.

   Allow 30 seconds before re-powering an instrument that has been switched off. If the power is switched more frequently than that, the turn-on delay may be longer (up to 20 seconds) as the internal software performs filesystem checks, or the instrument may remain unresponsive indefinitely.

2. OVERLOAD Indicator. When the instrument is powered, this indicator is normally green, indicating normal operation. If this indicator is yellow, an internal automatic overload protection circuit has been tripped. If the unit is overloaded (by operating at an exceedingly high duty cycle or by operating into a very low impedance), the protective circuit will disable the output of the instrument and turn the indicator light yellow. The light will stay yellow (i.e. output disabled) for about 5 seconds after which the instrument will attempt to re-enable the output (i.e. light green) for abOUT1 second. If the overload condition persists, the output will be disabled again (i.e. light yellow) for another 5 seconds. If the overload condition has been removed, the instrument will resume normal operation.

   This overload indicator may flash yellow briefly at start-up. This is not a cause for concern.

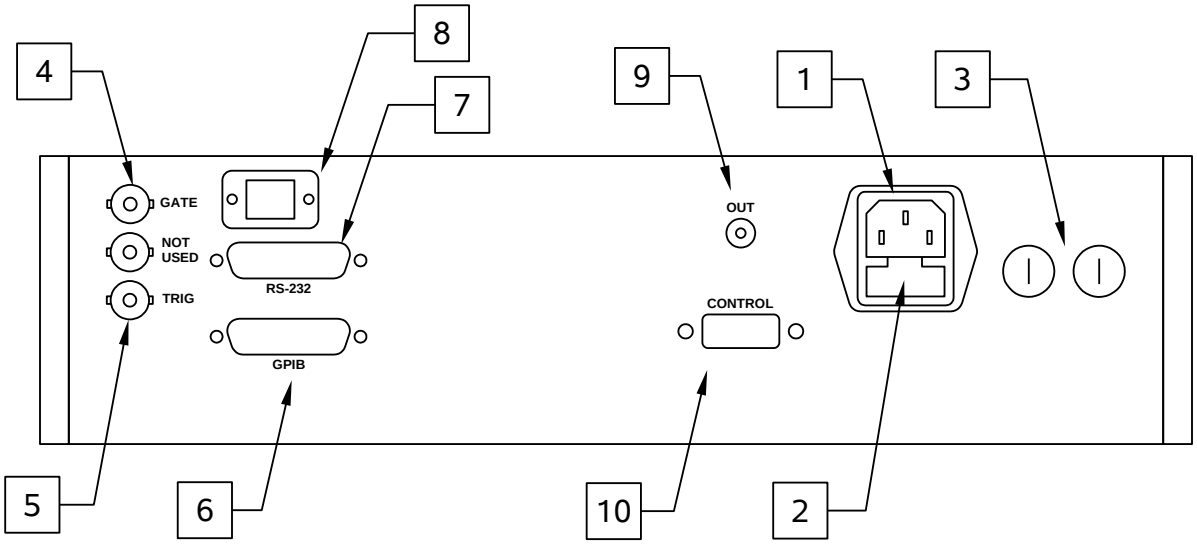
3. SYNC OUT. This connector supplies a SYNC output that can be used to trigger other equipment, particularly oscilloscopes. This signal leads (or lags) the main output by a duration set by the "DELAY" controls and has an approximate amplitude of +3 Volts to R_L > 50Ω with a pulse width of approximately 100 ns.

4. LIQUID CRYSTAL DISPLAY (LCD). This LCD is used in conjunction with the keypad to change the instrument settings. Normally, the main menu is displayed, which lists the key adjustable parameters and their current values. The “Programming Manual for -B Instruments” describes the menus and submenus in detail.

5. KEYPAD.

Control Name	Function
MOVE	This moves the arrow pointer on the display.
CHANGE	This is used to enter the submenu, or to select the operating mode, pointed to by the arrow pointer.
×10	If one of the adjustable numeric parameters is displayed, this increases the setting by a factor of ten.
÷10	If one of the adjustable numeric parameters is displayed, this decreases the setting by a factor of ten.
+/-	If one of the adjustable numeric parameters is displayed, and this parameter can be both positive or negative, this changes the sign of the parameter.
EXTRA FINE	This changes the step size of the ADJUST knob. In the extra-fine mode, the step size is twenty times finer than in the normal mode. This button switches between the two step sizes.
ADJUST	This large knob adjusts the value of any displayed numeric adjustable values, such as frequency, pulse width, etc. The adjust step size is set by the "EXTRA FINE" button. When the main menu is displayed, this knob can be used to move the arrow pointer.

REAR PANEL CONTROLS



Note: some connectors may be in different positions than shown above, depending on the exact combination of options ordered.

1. AC POWER INPUT. An IEC-320 C14 three-pronged recessed male socket is provided on the back panel for AC power connection to the instrument. One end of the detachable power cord that is supplied with the instrument plugs into this socket.

2. AC FUSE DRAWER. The two fuses that protect the AC input are located in this drawer. Please see the “FUSES” section of this manual for more information.

3. DC FUSES. These two fuses protect the internal DC power supplies. Please see the “FUSES” sections of this manual for more information.

4. GATE. This TTL-level (0 and +5V) logic input can be used to gate the triggering of the instrument. This input can be either active high or active low, depending on the front panel settings or programming commands. (The instrument triggers normally when this input is unconnected). When set to active high mode, this input is pulled-down to ground by a 1 kΩ resistor. When set to active low mode, this input is pulled-up to +5V by a 1 kΩ resistor.

5. TRIG. This TTL-level (0 and +5V) logic input can be used to trigger the instrument, if the instrument is set to triggering externally. The instrument triggers on the rising edge of this input. The input impedance of this input is 1 kΩ. (Depending on the length of cable attached to this input, and the source driving it, it may be desirable to add a coaxial 50 Ohm terminator to this input to provide a proper transmission line termination. The Pasternack (www.pasternack.com) PE6008-50 BNC feed-thru 50

Ohm terminator is suggested for this purpose.)

6. GPIB Connector. A standard GPIB cable can be attached to this connector to allow the instrument to be computer-controlled. See the “Programming Manual for -B Instruments” for more details on GPIB control.

7. RS-232 Connector. A standard serial cable with a 25-pin male connector can be attached to this connector to allow the instrument to be computer-controlled. Instruments with firmware versions of 5.00 or higher require a user name (“admin”) and a password (“default”, as shipped from the factory) when logging into a serial terminal session. See the “Programming Manual for -B Instruments” for more details on RS-232 control.

8. Network Connector. (Optional feature. Present on -VXI units only.) This Ethernet connector allows the instrument to be remotely controlled using the VXI-11.3, ssh (secure shell), telnet, and http (web) protocols. See the “Programming Manual for -B Instruments” for more details.

9. PULSE OUT CONNECTOR. This SMA connector provides the pulse output signal to the rise time filter. This output should be connected to the corresponding input on the rise time filter using the supplied SMA-to-SMA coaxial cable and SMA female-female adapter.

   ⚠ Caution: Voltages as high as 100V may be present on the center conductor of this output connector. Avoid touching this conductor. Connect to this connector using standard coaxial cable, to ensure that the center conductor is not exposed.

10. CONTROL Connector(s). Depending on the exact configuration of the instrument, one or two “CONTROL” connectors may be present on the back panel.

    If just one CONTROL connector is present, it will be a DB-9 female connector.

    If two CONTROL connectors are present, one will be a DB-9 female connector and one will be a DB-25 female connector. Only one of the two connectors should be used at a time. Use the one that matches the CONTROL connector on the test jig being used (i.e., DB-9 or DB-25).

    The mainframe CONTROL connector should be connected to the corresponding connector on the test jig using the supplied cable. This cable contains the safety interlock signals that ensure that the test jig lid is closed.

    For DB-9 cables, the pinout is as follows:

    Pin 1 - To test jig switch 1.
    Pin 2 - To test jig switch 2.
    Pin 3 - N/C.
    Pin 4 - N/C.
    Pin 5 - Ground.

Pin 6 - To test jig switch 1.
Pin 7 - To test jig switch 2.
Pin 8 - N/C.
Pin 9 - Safety sensor power supply (+15V through 680 Ohms).

When the test jig lid is safely closed, Pin 1 is shorted to Pin 6, and Pin 2 is shorted to Pin 7.

For DB-25 cables, the pinout is as follows:

Pin 1 - To test jig switch 1.
Pin 2 - To test jig switch 2.
Pin 3 - N/C.
Pin 4 - N/C.
Pin 5 - Ground.
Pin 6 - Ground.
Pin 7 - Ground.
Pin 8 - +5V DC.
Pin 9 - +5V DC.
Pin 10 - pin socket select signal (TTL).
Pin 11 - pin socket select signal (TTL).
Pin 12 - pin socket select signal (TTL).
Pin 13 - pin socket select signal (TTL).
Pin 14 - To test jig switch 1.
Pin 15 - To test jig switch 2.
Pin 16 - N/C.
Pin 17 - Safety sensor power supply (+15V through 680 Ohms).
Pin 18 - N/C.
Pin 19 - Ground.
Pin 20 - +5V DC.
Pin 21 - +5V DC.
Pin 22 - pin socket select signal (TTL).
Pin 23 - pin socket select signal (TTL).
Pin 24 - pin socket select signal (TTL).
Pin 25 - pin socket select signal (TTL).

When the test jig lid is safely closed, Pin 1 is shorted to Pin 14, and Pin 2 is shorted to Pin 15.

TIMING CONTROL

BASIC TIMING CONTROL

This instrument can be triggered by its own internal clock or by an external TTL trigger signal. In either case, two output channels respond to the trigger: OUT and SYNC. The OUT channel is the signal that is applied to the load. Its amplitude and pulse width are variable. The SYNC pulse is a fixed-width TTL-level reference pulse used to trigger oscilloscopes or other measurement systems. When the delay is set to a positive value the SYNC pulse precedes the OUT pulse. When the delay is set to a negative value the SYNC pulse follows the OUT pulse.

These pulses are illustrated below, assuming internal triggering and a positive delay:

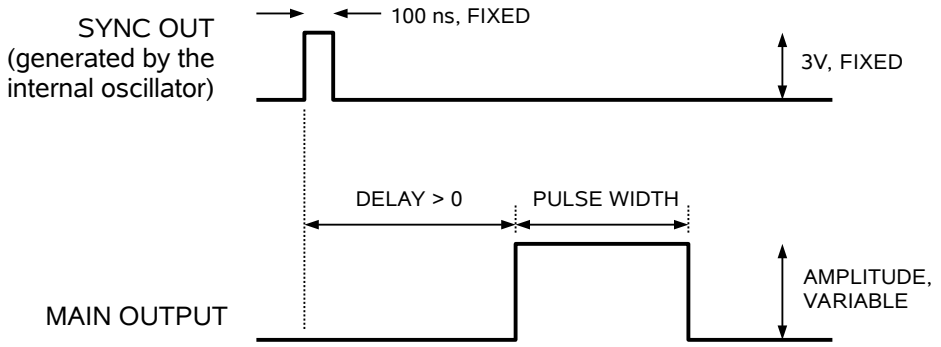


Figure A

If the delay is negative, the order of the SYNC and OUT pulses is reversed:

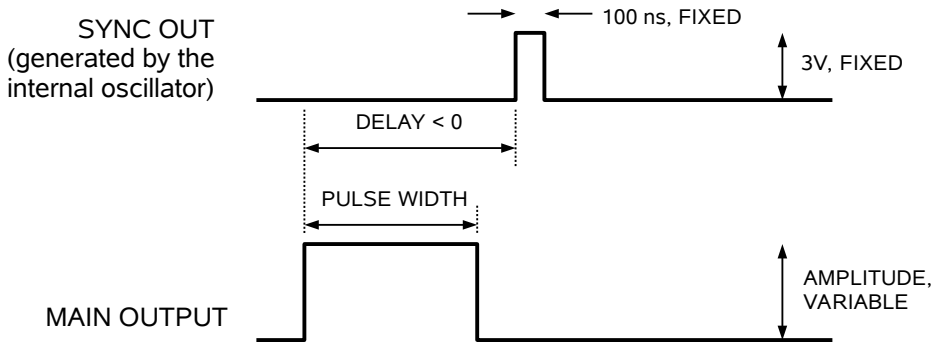


Figure B

The next figure illustrates the relationship between the signal when an external TTL-level trigger is used:

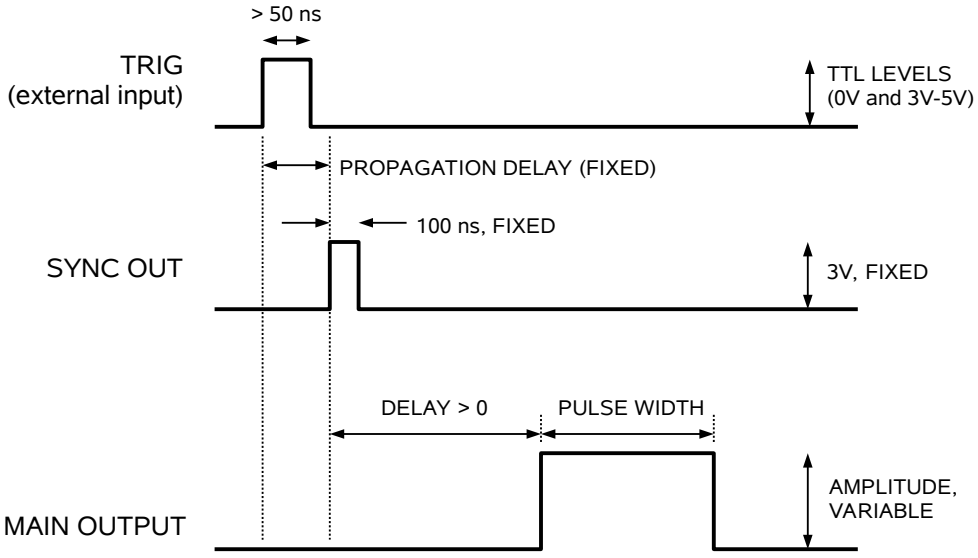


Figure C

As before, if the delay is negative, the order of the SYNC and OUT pulses is reversed.

TRIGGER MODES

This instrument has four trigger modes:

- Internal Trigger: the instrument controls the trigger frequency, and generates the clock internally.
- External Trigger: the instrument is triggered by an external TTL-level clock on the back-panel TRIG connector.
- Manual Trigger: the instrument is triggered by the front-panel “SINGLE PULSE” pushbutton.
- Hold Trigger: the instrument is set to not trigger at all.

These modes can be selected using the front panel trigger menu, or by using the appropriate programming commands. (See the “Programming Manual for -B Instruments” for more details.)

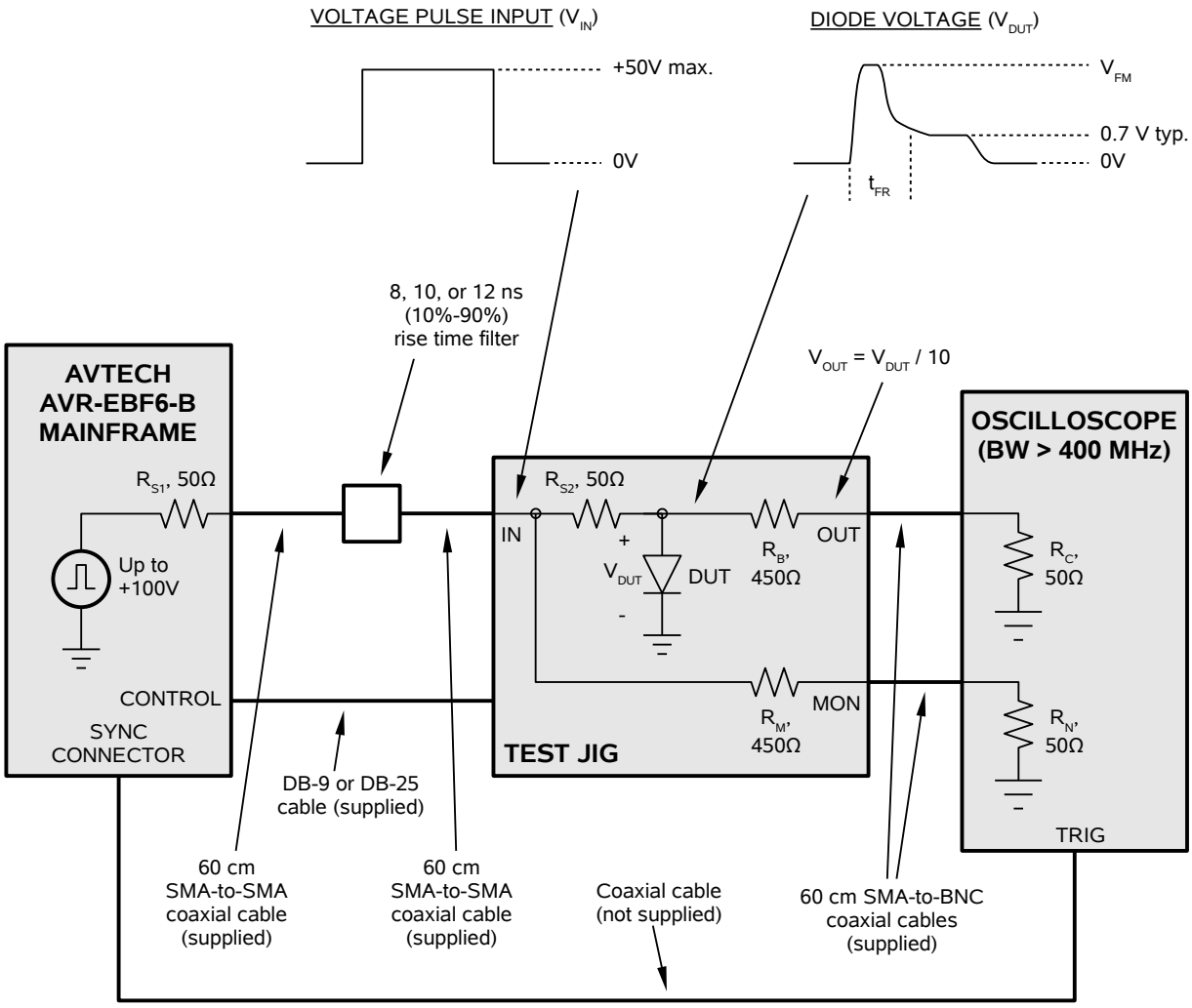
GATING MODES

Triggering can be suppressed by a TTL-level signal on the rear-panel GATE connector. The instrument can be set to stop triggering when this input high or low, using the front-panel gate menu or the appropriate programming commands. When gated, the output

will complete the full pulse width if the output is high, and then stop triggering. Pulses are not truncated.

BASIC AMPLITUDE CONTROL

The basic test arrangement for the AVR-EBF6-B is shown in the figure below:



The mainframe connects to the rise time filter using a 60 cm length of SMA-to-SMA coaxial cable.

The output of the filter connects to the test jig using another 60 cm length of SMA-to-SMA coaxial cable.

A DB-9 (or DB-25, depending on the jig provided) control cable connects the mainframe to the test jig, to control the safety interlocks.

The test jig main output is fed into the 50 Ohm input of an oscilloscope by a 60 cm length of BNC-to-SMA coaxial cable, as is the monitor output.

The SYNC output of the mainframe should be used to trigger the oscilloscope.

⚠ A 50 Ohm resistance (R_C in the diagram above) must be connected to ground on the output. This can be a discrete resistor, a feed-through terminator, or the input impedance of an oscilloscope (the latter method is shown in the diagram). If a high-speed sampling oscilloscope is used, the input should be protected by adding attenuator on the input.

The 450 Ohm resistance in series with the test jig output and the 50 Ohm input impedance of the oscilloscope form a 10:1 voltage, so the measured voltage is:

$$V_{OUT} = V_{DUT} / 10$$

The monitor output is similarly divided by a factor of 10, so that:

$$V_{MON} = V_{IN} / 10$$

The monitor output is provided so that the user may determine the starting point of the transient.

SETTING THE AMPLITUDE LEVELS

The amplitude pulse may be set from the front panel of the instrument, or by computer command. This amplitude is expressed in terms of the voltage present on the test jig input.

The amplitude is related to the forward diode current by:

$$I_F \approx (V_{IN} - V_{DUT}) / 50\Omega$$

where V_{DUT} is the forward voltage drop of the diode (typically 0.7V for the classic silicon PN junction diode, and usually somewhat lower for a Schottky diode).

For instance, if the desired forward current amplitude is 500 mA, the amplitude should be set at 25.7V, so that (25.7V – 0.7V) / 50Ω = 500 mA. It may be necessary to adjust the amplitude iteratively to obtain the desired I_F, since V_{DUT} may not be known in advance.

AMPLITUDE ACCURACY

⚠ Due to the variations in V_F as a function of operating conditions, the amplitude settings *should not be relied upon for any degree of accuracy*. Instead the voltage at the OUT terminal on the test jig should be monitored with a calibrated oscilloscope.

R_B can be measured directly on the test jig (with the test jig disconnected) to determine calibrated relationships, if desired. R_C is provided by the user, and can be calibrated as required.

INCORRECT ORIENTATION

The instrument and the DUT will not be damaged if the diode is installed with the incorrect orientation (i.e., with the anode and cathode reversed). However, incorrect waveforms will be generated,

CABLE LENGTHS

The cable lengths are not critical. They may be increased or decreased as desired.

The cables connecting the OUT and MON signals to the oscilloscope should have identical lengths, to avoid introducing timing skews.

ACCESSIBLE VOLTAGES

The mainframe provides pulsed voltages of up to 100V to the test jig. For this reason, the output is automatically disabled when the test jig lid is open. The lid must be closed to obtain measurements.

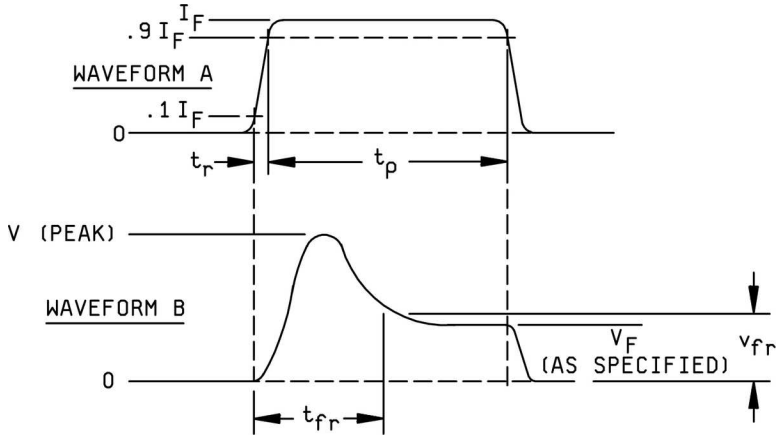
⚠ Shielded cabling should be used for all connections to the "IN" and "OUT" terminals on the test jig, and the "OUT" connector on the mainframe.

⚠ When used properly (with R_C = 50 Ohms), the maximum voltage on the OUT terminal will be < 1V, approximately. However, if R_C is not connected and the DUT is not installed, the maximum voltage will at the OUT terminal may be as high as 100V. You may need to consider whether this scenario would damage your oscilloscope, and take appropriate precautions.

BASIC MEASUREMENT THEORY

The basic procedure for measuring the forward recovery voltage and time is described in method 4026.3 of MIL-STD-750E. The user should familiarize themselves with this method before using this instrument.

The basic parameters are shown in Figure 4026-1 of MIL-STD-750E, reproduced in part here:



"Waveform B" in this figure is the voltage across the DUT, V_{DUT}. This is related to the OUT signal on the test jig by:

$$V_{OUT} = V_{DUT} / 10.$$

"Waveform A" in this figure is the current through the DUT, I_F. This is related to the OUT and MON signals on the test jig by:

$$I_F \approx (V_{IN} - V_{DUT}) / 50\Omega$$

$$I_F \approx (10 \times V_{MON} - 10 \times V_{OUT}) / 50\Omega$$

The above figure shows t_{fr} as the time between 0.1 I_F and V_{fr}.

Unfortunately, the text also says t_{fr} is "measured from the time forward voltage becomes positive to the time that forward voltage recovers to a specified vfr", which is slightly different. The "time forward voltage becomes positive" is before the time where 0.1 I_F is reached.

In practice, it is impossible to measure the "time forward voltage becomes positive" repeatably. 0.1 I_F is a much easier time to identify and measure in an automated system.

In the test results included in later sections, the approximation that 0.1 I_F occurs at 0.1 V_{IN} (or 0.1 V_{MON}) is used to simplify measurements. This provides conservative results,

since 0.1 I_F actually occurs slightly after 0.1 V_{IN}. This will slightly increase the measured t_{FR} value.

If you prefer to not use this approximation, you will need to use the math functions of your oscilloscope to identify 0.1 ($V_{MON} – V_{OUT}$), rather than 0.1 V_{MON}.

TEST JIG MECHANICAL ASPECTS

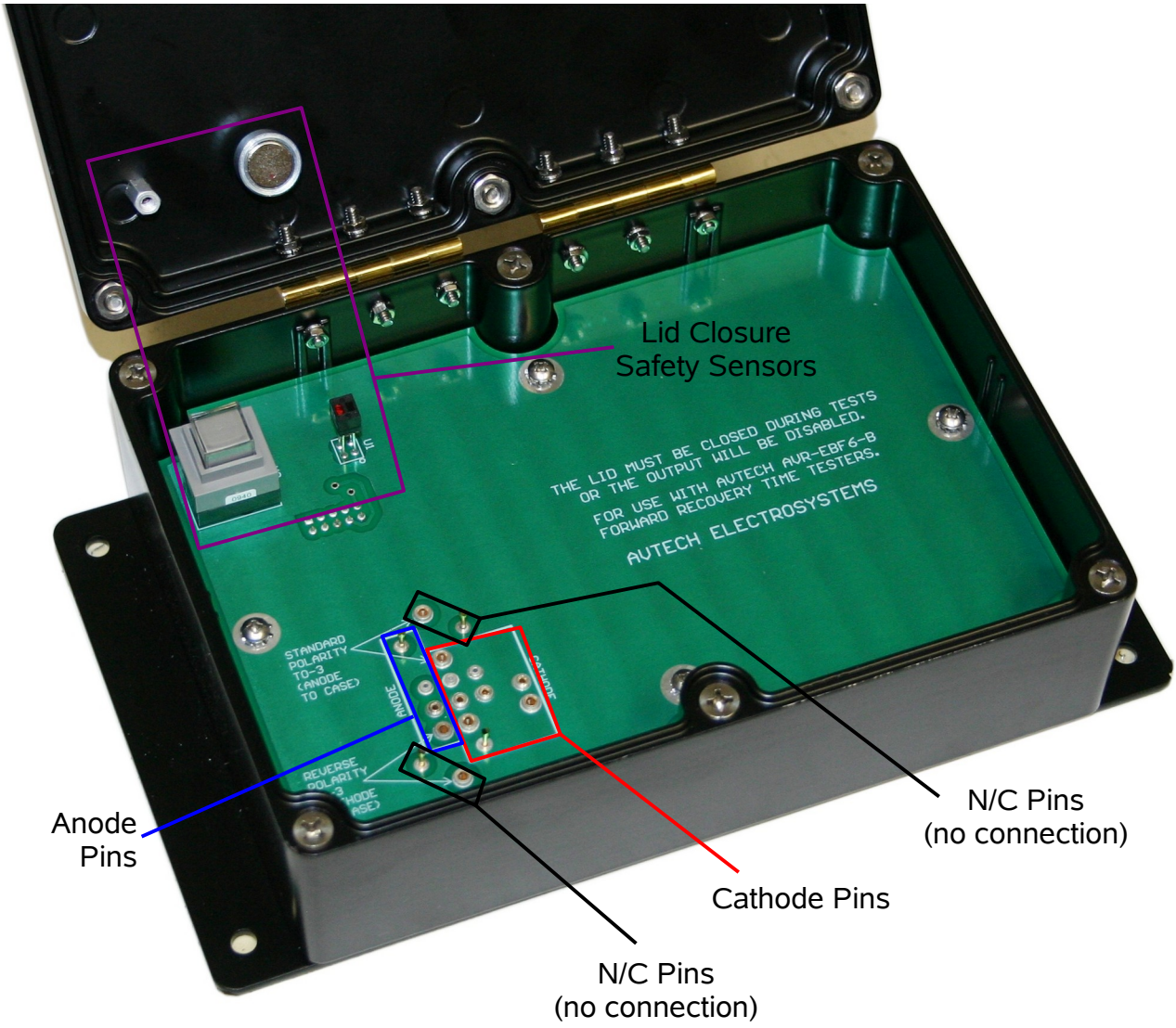
ALL TEST JIGS

The IN, MON, OUT, and CONTROL connectors are on the rear of the jig, below the hinges:

AVX-TFR-MIX TEST JIG

One AVX-TFR-MIX test jig is normally supplied with the mainframe, unless the customer has requested a different or additional test jigs.

The AVX-TFR-MIX test jig accepts a range of through-hole and axial devices, using pin sockets and spring-loaded pins. It is intended for use with diodes in DO-41, TO-220, DO-204AR, TO-3 or similar packages. A photo of the arrangement is shown below:



The instrument and the DUT will not be damaged if the diode is installed with the incorrect orientation (i.e., with the anode and cathode reversed). However, incorrect waveforms will be generated.

The procedure for inserting most axial and TO-220 packages is straightforward. Simply insert the DUT between one of the Anode pin sockets (in the blue area above) and one of the Cathode sockets (in the red area above). Select the sockets with the most appropriate hole size, and try to minimize all lead lengths, to minimize parasitic inductance.

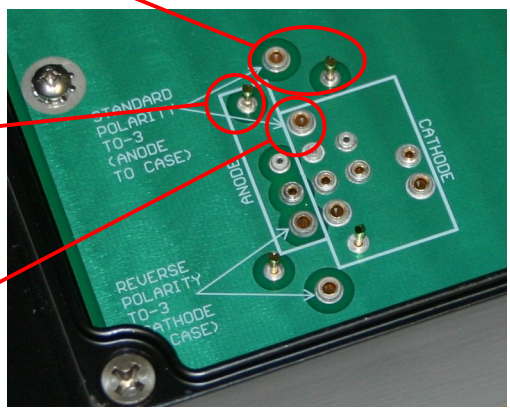
This jig will also accommodate a number of TO-3 configurations, outlined below. If the case is connected to the anode, and the pin(s) are used for the cathode, the arrangement shown below must be used:

For TO-3 packages with Case = Anode

This socket and spring pin provide mechanical support only. They are not electrically active.

This spring pin must contact the underside of the case. It provides the anode connection.

The cathode pin of interest must be inserted into this socket. For dual-diode devices, rotate the TO-3 package so that the desired diode cathode is inserted here.



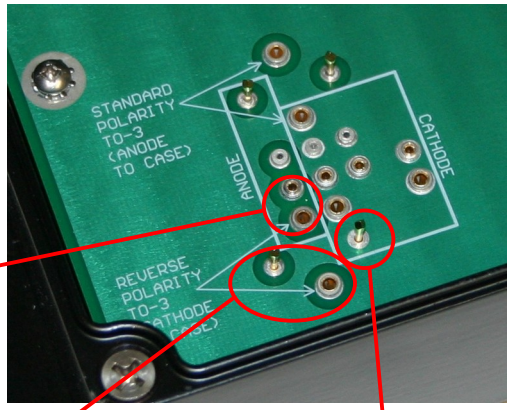
If the case is connected to the cathode, and the pin(s) are used for the anode, the arrangement shown below must be used:

For TO-3 packages with Case = Cathode

The anode pin of interest must be inserted into this socket. For dual-diode devices, rotate the TO-3 package so that the desired diode anode is inserted here.

This socket and spring pin provide mechanical support only. They are not electrically active.

This spring pin must contact the underside of the case. It provides the cathode connection.



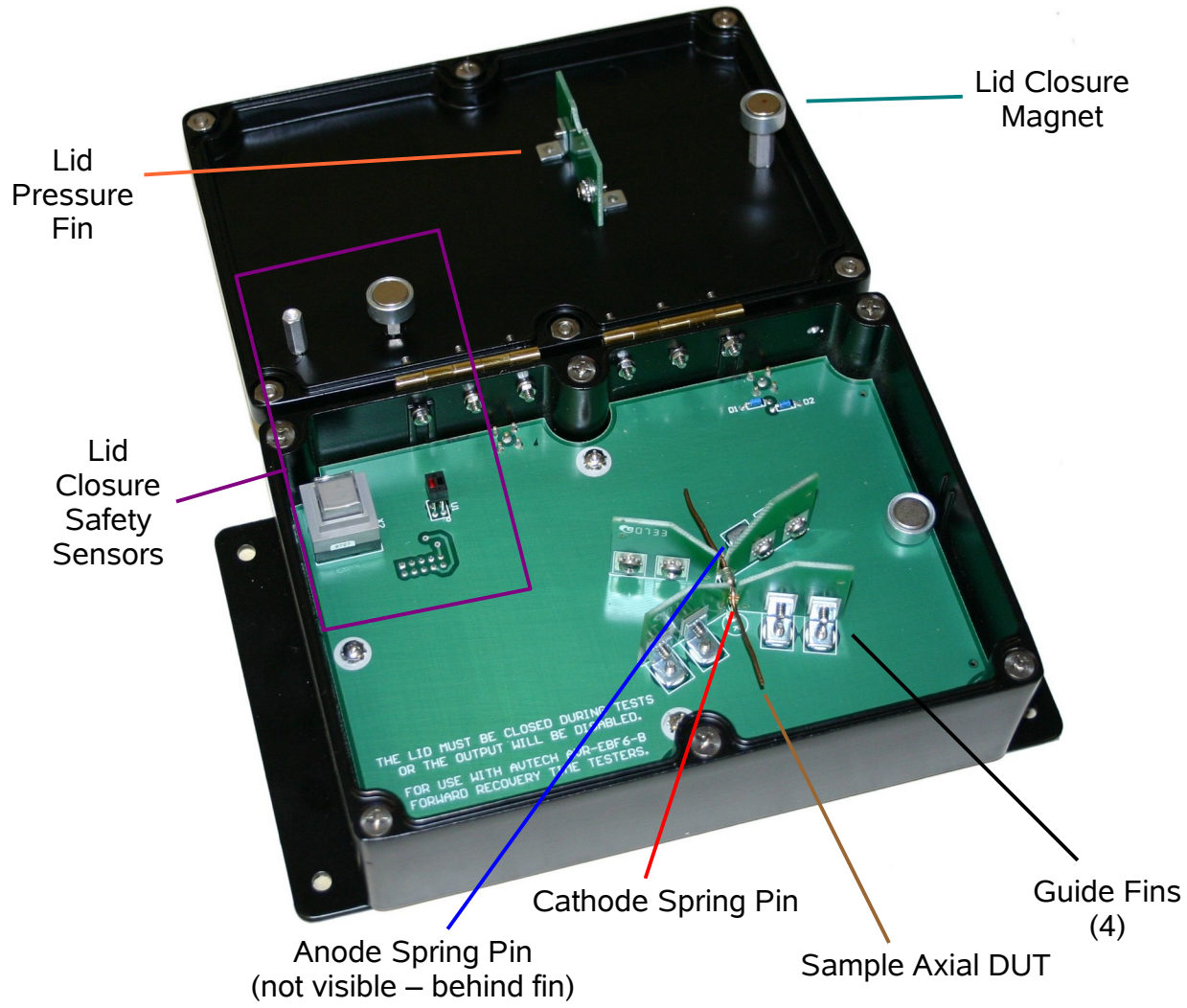
AVX-TFR-ANB TEST JIG

If the AVR-EBF6-B has been ordered with the -ANB option, an AVX-TFR-ANB test jig replaces the standard AVX-TFR-MIX test jig. The AVX-TFR-ANB test jig may also be ordered separately. In contrast to the AVX-TFR-MIX, no lead bending is required.

The AVX-TFR-ANB test jig accepts two types of packages:

- DO-41 (0.205" x 0.107" body, maximum)
- Microsemi Axial Type E (0.185" x 0.135" body, maximum)

The DUT is installed in the test jig by dropping it over the area marked “DUT” on the test jig PCB. Four “fins” guide the DUT into the correct position between two spring-loaded test pins. When the hinged lid is closed, a fifth “fin” attached to the underside of the lid presses the DUT against the spring-loaded pins, to ensure good electrical contact. A DUT is shown in position in the photo below (with the lid open):



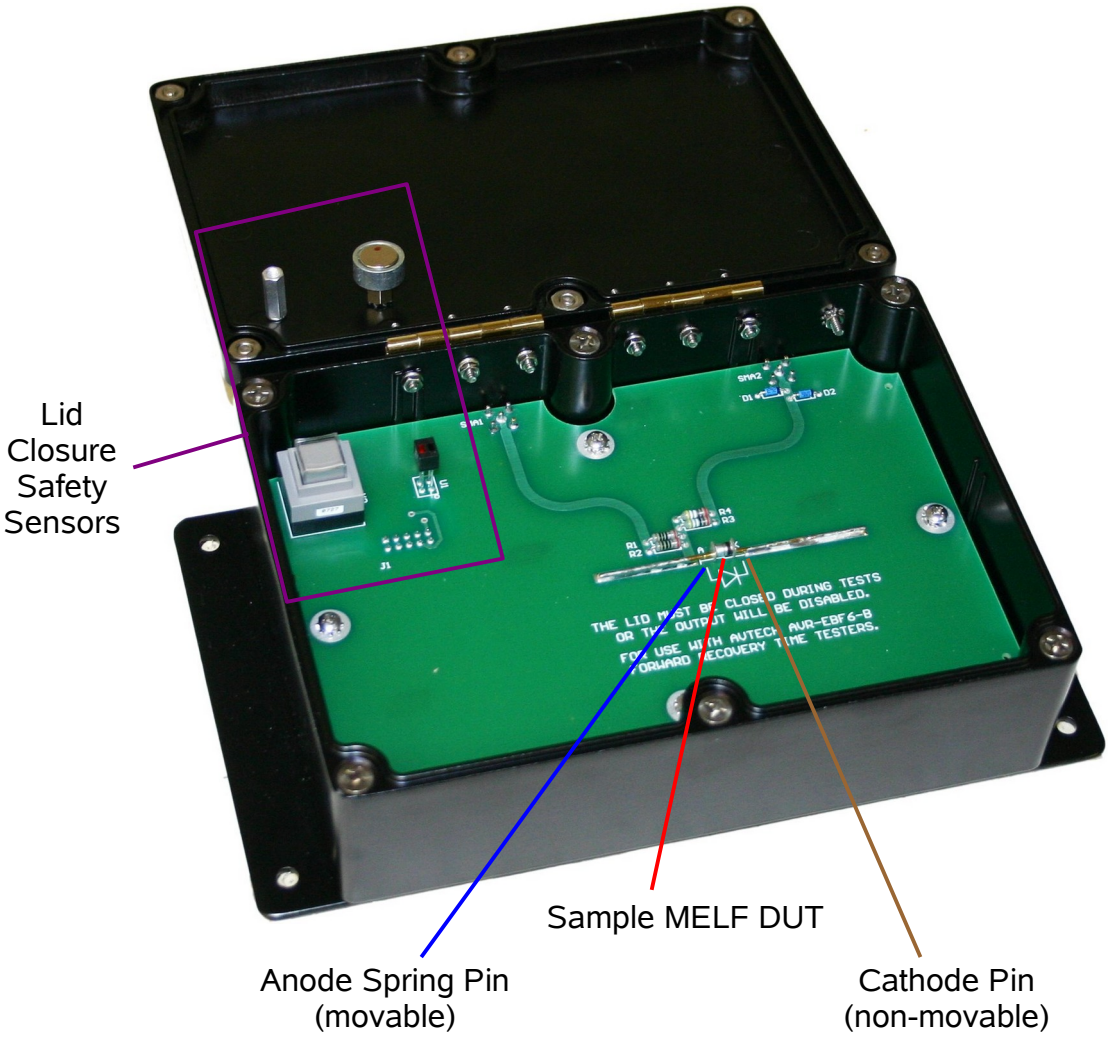
The instrument and the DUT will not be damaged if the diode is installed with the incorrect orientation (i.e., with the anode and cathode reversed). However, incorrect waveforms will be generated.

When closed, the lid is held is place by a magnetic latch. To open the lid, simply pull upwards on the handle at the front of the lid.

Over time, the “lid pressure fin” may become worn down, resulting in poor DUT contact with the spring pins. Four replacement fins are included with each AVX-TRR-ANB, for this reason.

AVX-TFR-MELF

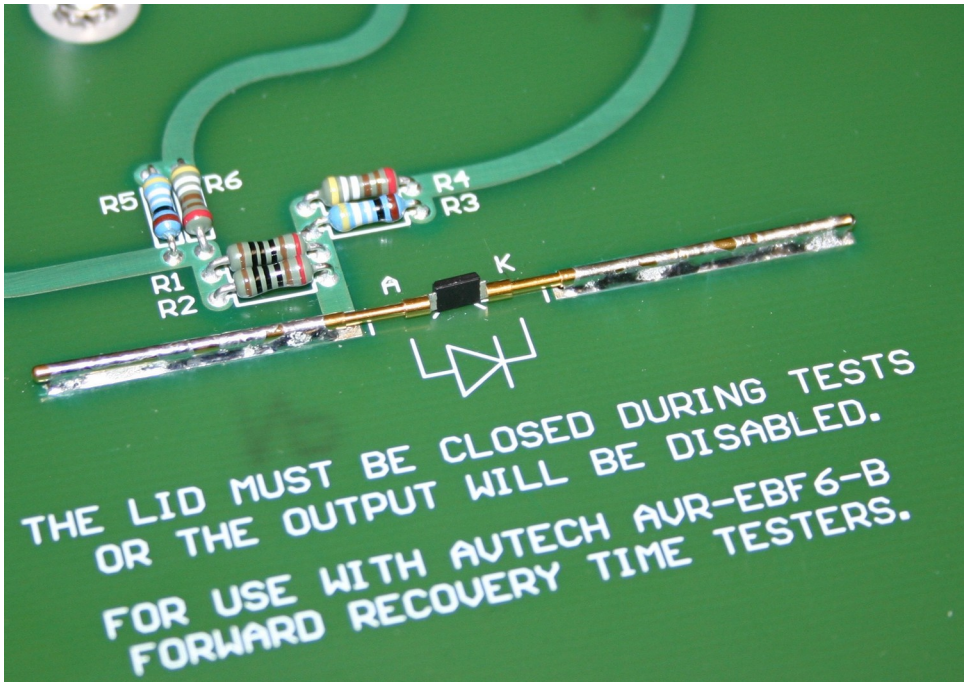
The AVX-TFR-MELF jig, which may be ordered separately, accepts MELF packages as shown below:



The anode spring pin must be pushed back to make room for the DUT. The cathode pin is not movable (the spring action has been disabled, to minimize series inductance).

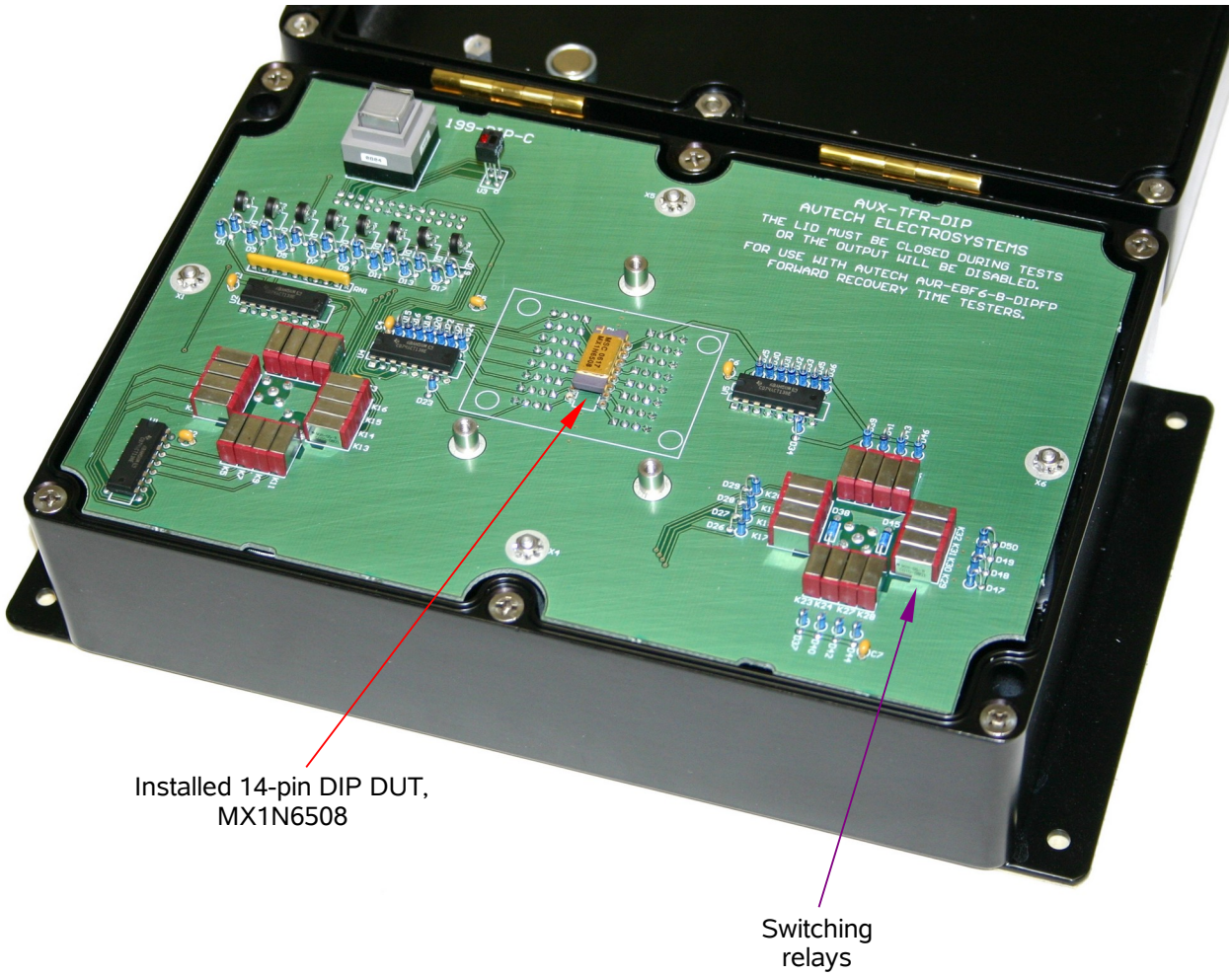
AVX-TFR-MELF-NXPA

This test jig is similar to the standard AVX-TFR-MELF jig described in the previous section, except that it is intended for use with SOD123W, SOD128, SOD123F, SOD323F, and similar surface-mount packages. The DUT is installed, using tweezers, between the two opposing flat-headed spring pins. For test purposes, it is best to install the DUT so that the flat leads are perpendicular to the circuit board, rather than parallel to it. This makes it easier to position the DUT with tweezers, and makes it easier to verify that the spring pin heads are making contact with the leads. A photo of an installed DUT is shown below:



AVX-TFR-DIPFP, FOR DIP PACKAGE TESTS

The AVX-TFR-DIPFP can be used to test DIP packages or military-style flat-packs. When testing DIP packages, the DIP-to-flat-pack adapter is removed. The basic test jig is shown below:



The device under test (DUT) is installed in the array of 16 pin sockets in the middle of the PCB. Pin 1 is towards the rear of the jig (the hinged side). A DIP extractor tool is provided to assist in removing installed DUTs.

The jig contains a very large number of relays and (hidden) coaxial cables for switching signals between the 16 pins. These relays are controlled from the front panel by the “Anode” and “Cathode” menus. These menus should be used to select the diode of interest inside the DIP package.

Computer commands can also be used to select the pins of interest. For instance, if you wish to test a diode which has its anode on pin 4 and its cathode on pin 8, send these two commands:

route:close (@anod(4))
route:close (@cath(8))

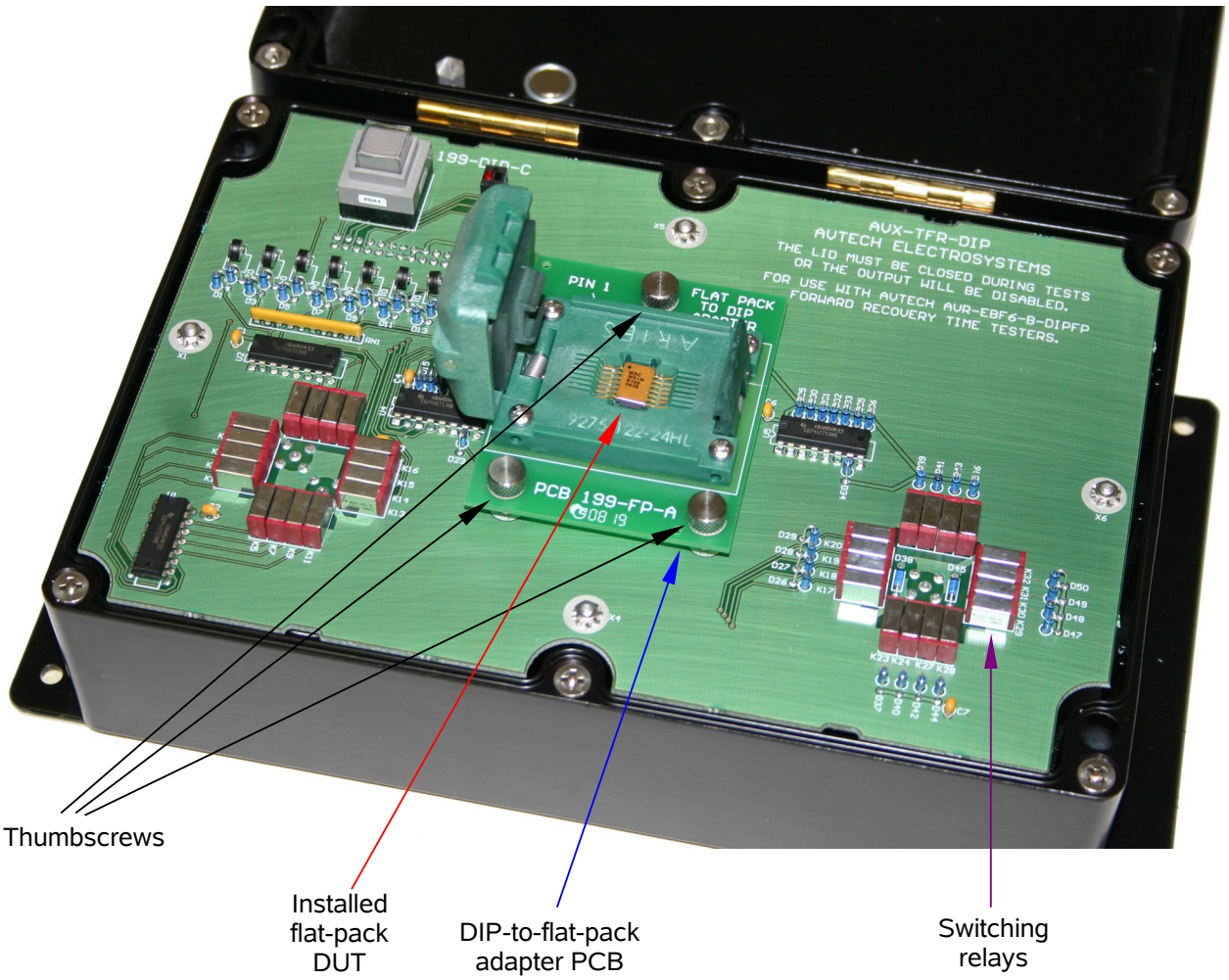
The brackets and the “@” symbol are mandatory (as specified by SCPI, “Standard Commands for Programmable Instrumentation”).

The pin socket array will accept DIP packages with up to 16 pins. If your DUT has fewer than 16 pins, install the DUT such that pin 1 is towards the rear of the jig (the hinged side). The pin numbering used in the Anode and Cathode menus (and the route:close command) is based on the 16 pin package. You will need to adjust for this when using non-16-pin packages. For instance, if you insert an 8 pin DIP, pins 1-8 of the package will actually be installed in pin sockets 1-4 and 13-16.

AVX-TFR-DIPFP, FOR FLAT-PACK TESTS

A DIP-to-flat-pack adapter can be installed in the AVX-TFR-DIPFP to allow it to accept military-style flat-packs with up to 16 pins. The adapter has a clamshell-socket for the flat-pack on top, and 16 pins on the bottom. The 16 pins insert into the 16 pin sockets on the AVX-TFR-DIPFP (that is, where a DIP DUT would go).

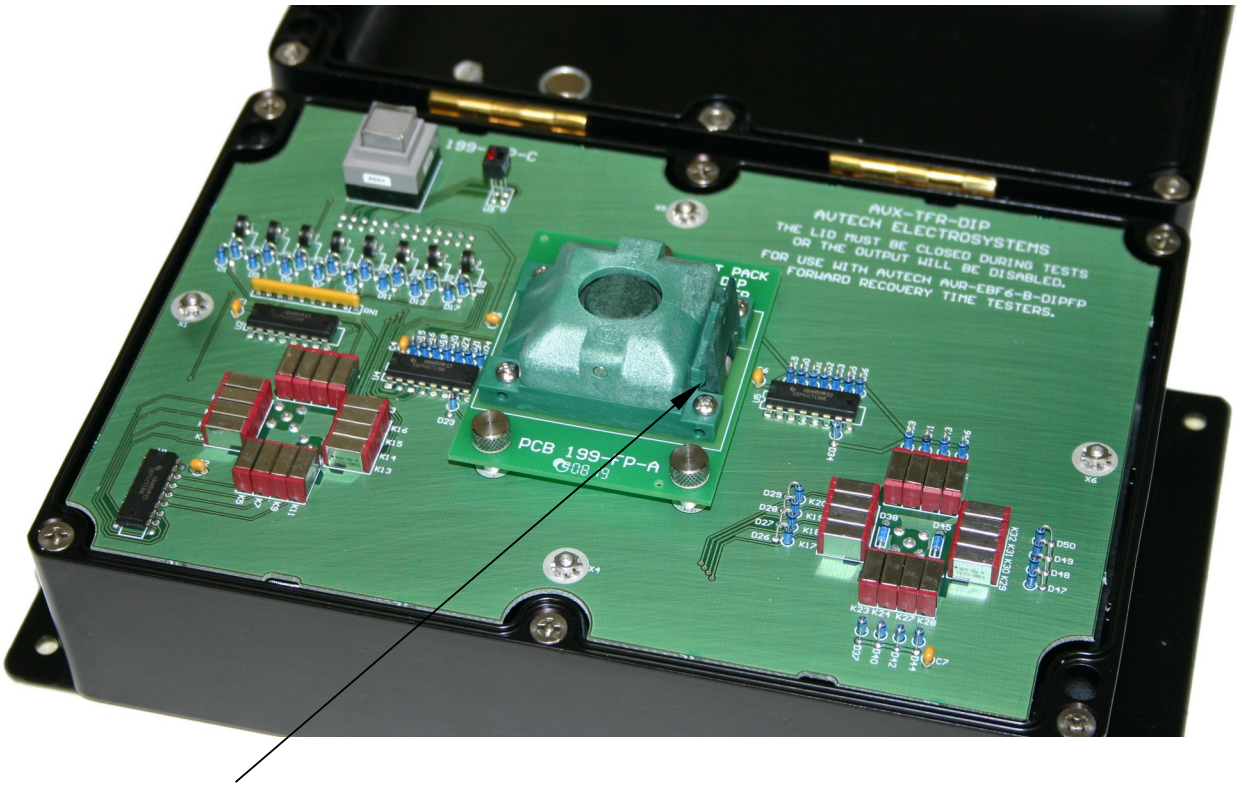
To install the adapter, gently insert the 16 pins into the 16 pin sockets, and then secure the adapter using the 3 supplied 4-40 thumbscrews, as shown below.



The adapter will accept flat-packs with up to 16 pins. If your DUT has fewer than 16 pins, install the DUT such that pin 1 is towards the rear of the jig (the hinged side). The pin numbering used in the Anode and Cathode menus (and the route:close command) is based on the 16 pin package. You will need to adjust for this when using non-16-pin packages. For instance, if you insert an 8 pin DIP, pins 1-8 of the package will actually be installed in pin sockets 1-4 and 13-16.

Note that the clamshell has a “rocker” bracket on the top, to assist in positioning the DUT inside the clamshell socket. When the clamshell is closed, the rocker bracket presses the flat-pack pins against an array of miniature vertical spring pins, to make electrical contact. The electrical paths are very short.

Once the DUT is installed inside the open clamshell, the clamshell must be latched shut:



Clamshell latch,
closed for testing

The main black hinged lid must also be closed to enable the output.

The procedure for controlling the active pins is the same as described in the previous section (for DIP packages).

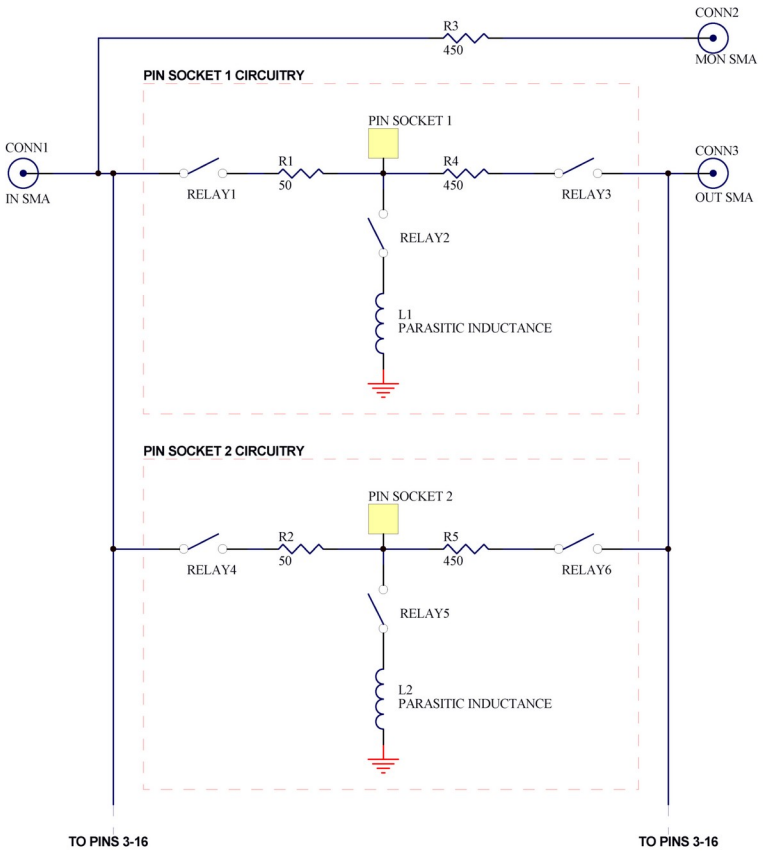
AVX-TFR-DIPFP INDUCTANCE NULLING

The AVX-TFR-DIPFP contains 48 individual relays to switch signals – 3 per pin socket. For each pin socket, one relay connects to the input signal, one relay connects to the output signal, and one relay connects to ground.

When a pin socket has been configured as an anode, the input and output relays close and the ground relay opens.

When a pin socket has been configured as a cathode, the input and output relays open and the ground relay closes.

This general arrangement is illustrated below:



The relays that connect to the IN SMA are in series with a 50 Ohm resistance, and the OUT relays are in series with 450 Ohm resistances. The impedance of the parasitic inductance associated with these relays is negligible compared to the impedance of the series resistances. These inductances may be ignored.

However, the ground-shorting relays do not have any series resistance. Any inductive voltage that appears in the relay's parasitic inductance (L1 and L2 above) will appear on the output waveform, and will appear to increase VF slightly.

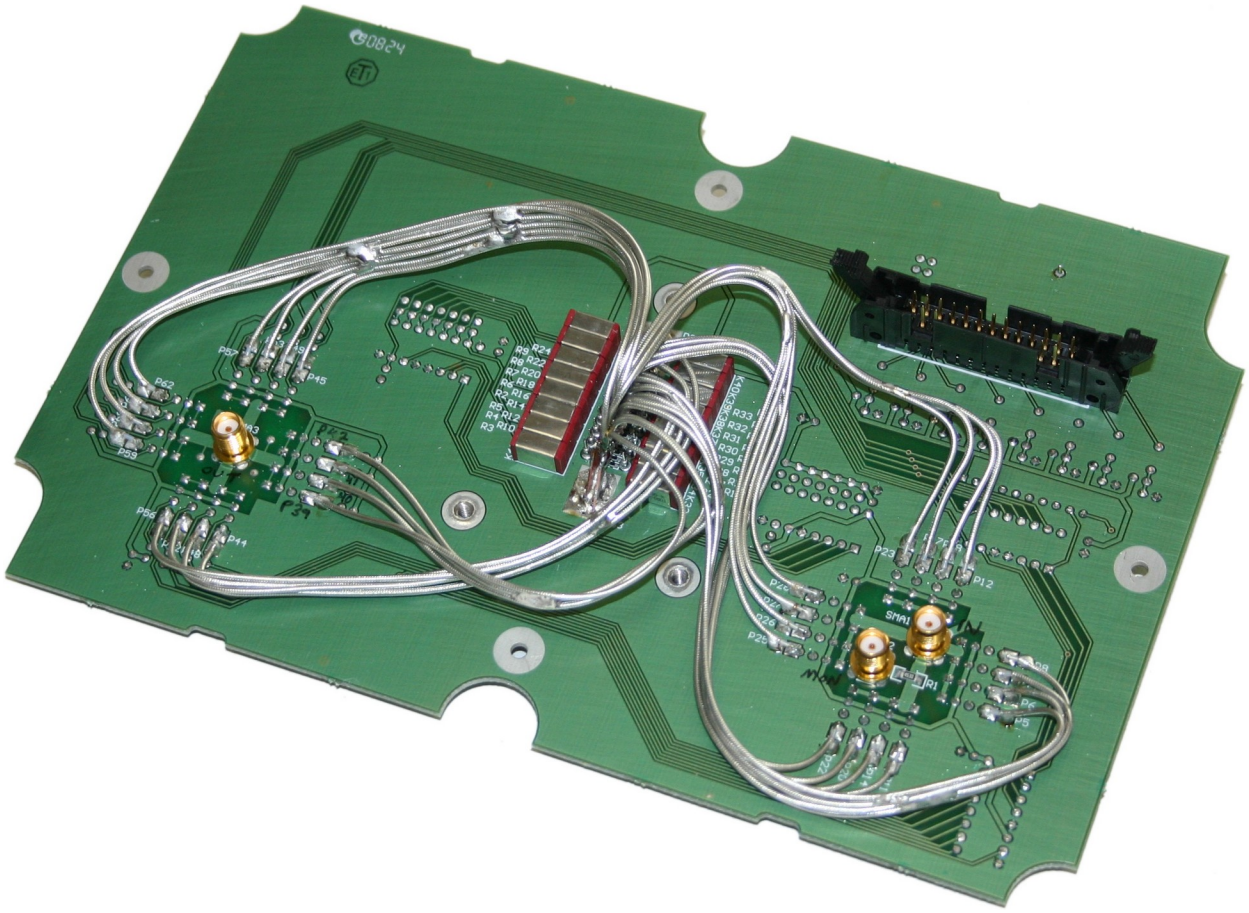
This is not a large effect – errors on the order of 0.2V per 100 mA are typical. This is may be problematic for a certain class of ultra-high-performance (high speed, low recovery time) devices. Fortunately, it is easy to compensate for this inductance. If you need to measure a diode that has its anode on pin 1 and its cathode on pin 2, first set the amplitudes and pin settings as you normally would, and record your waveform (waveform “A”).

Then, set the front-panel “ANODE” and “CATHODE” settings both to the actual cathode pin. That is, ANODE = CATHODE = 2. Repeat the measurement. This will close all three relays associated with the pin. The only output signal will be the voltage due to the ground relay inductance. Record this waveform (“B”).

Subtract waveform “B” from waveform “A”, to generate waveform “C”. Perform the actual recovery time measurements based on “C”. This will remove the effect of the inductance.

Real results illustrating this calculation are given in the “TYPICAL RESULTS – DIPS AND FLAT-PACKS” section later in this manual.

The grounding relays are located on the bottom side of the test jig (along with the miniature coaxial cables), very close to the pin sockets, as shown below:



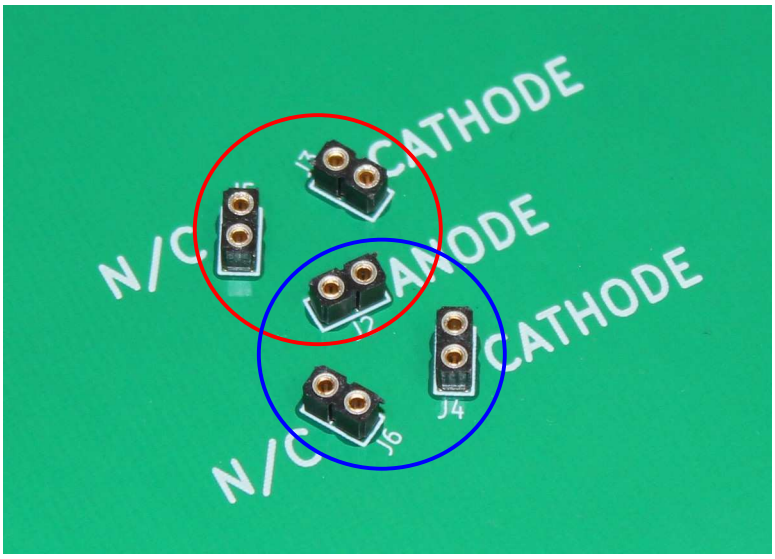
AVX-TFR-SOT23B

The AVX-TFR-SOT23B test jig provides an arrangement of sockets that will accept a small daughterboard. Three-pin SOT-23 devices may be soldered to the daughterboard. The daughterboard may be inserted into the sockets in six different orientations, permitting any combination of pins to be assigned as the anode and the cathode. One of the three device pins will be unused – however, footprints for jumpers are provided on the daughterboard to permit pins to be shorted together. For example, if the DUT is actually a MOSFET whose body diode needs to be characterized, then the gate pin is normally shorted to the source pin.

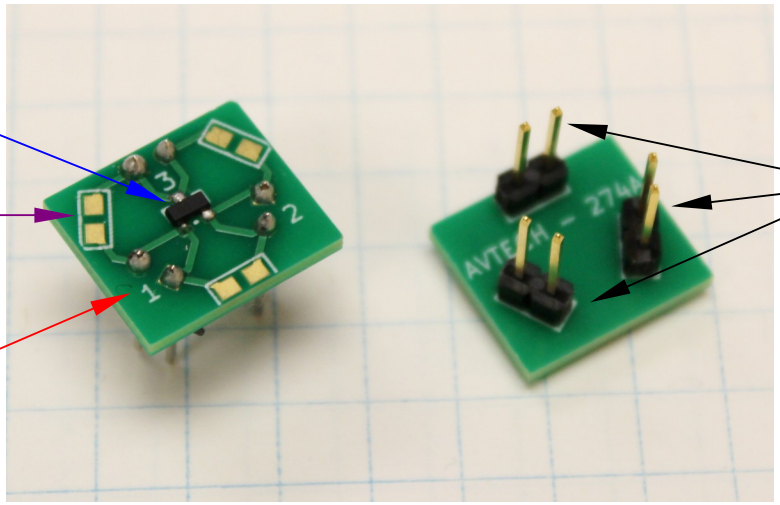
The basic jig, without a daughterboard, is shown below:

Five pairs of pin sockets are located near the center of the jig. The anode signal is present on the central pair. The cathode signal is present on two pairs, on the right side (they are wired in parallel). Two pairs, on the left side, are unconnected.

The daughterboard may be installed in two positions, using three of the five pairs at a time. The two positions are shown below:



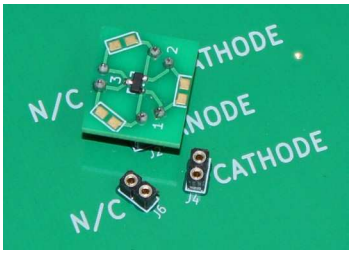
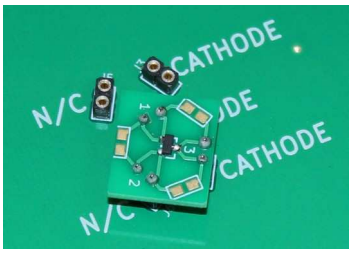
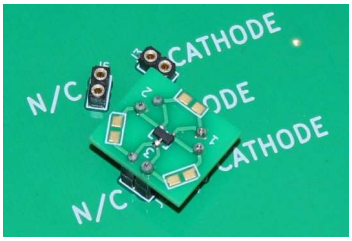
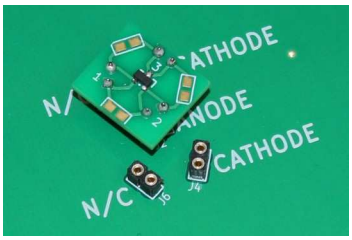
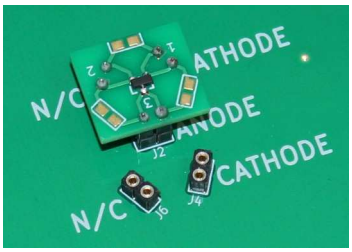
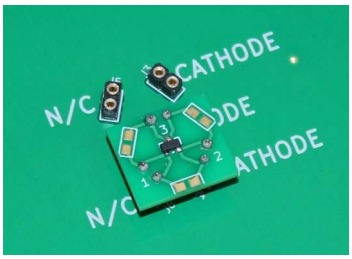
The top and bottom sides of the daughterboard are shown below:



The three pin post pairs are labeled “1”, “2”, and “3” on the top side, corresponding to the pin number of the SOT23 footprint that the pair connects to. Both posts in the pair are connected to the same pin.

The user will need to select one of the two possible positions, and one of three possible rotations, to ensure that the correct pin is connected to the anode signal, and the correct pin is connected to the cathode signal. The two positions and three rotations provide six possibilities.

Simple adjust the positioning of the daughterboard until the correct pin number is over the “ANODE” socket, and the correct pin number is over one of the two possible “CATHODE” sockets. The choices are summarized in the table below:

Pin Number of Anode	*Pin Number of Cathode*	*Unused Pin**	*Photo*
1	2	3	
1	3	2	
2	1	3	
2	3	1	
3	1	2	
3	2	1	

* The unused pin may be shorted to another pin, using the provided jumper footprints.

Heavy usage may wear out the pin sockets or the associated soldering. Replacement pin sockets are available from Mill-Max (https://www.mill-max.com), part number 834-43-002-10-001000.

The posts used on the AVX-TFR-SOT23B daughterboard are AMP part number 4-103321-0-02 (or a trimmed portion of part number 4-103321-0).

The Gerber and drill CAM files for the daughterboard are available for download here:

http://www.avtechpulse.com/semiconductor/avr-eb2a/#support_files

The user may wish to produce additional daughterboards as needed.

AVX-TFR-SOT23B INDUCTANCE NULLING

The jig and daughterboard arrangement does introduce some parasitic inductance. This is not a large effect – errors on the order of 0.2V per 100 mA are typical. This is may be problematic for a certain class of ultra-high-performance (high speed, low recovery time) devices.

Fortunately, it is easy to compensate for this inductance. With a diode DUT installed, record your waveform (waveform “A”) in the normal manner.

Then, repeat the test with a zero Ohm jumper installed on a daughterboard, using the same anode/cathode pads as were used with the real DUT. The only output signal will be the voltage due to the parastic inductance. Record this waveform (“B”).

Subtract waveform “B” from waveform “A”, to generate waveform “C”. Perform the actual recovery time measurements based on “C”. This will remove the effect of the inductance.

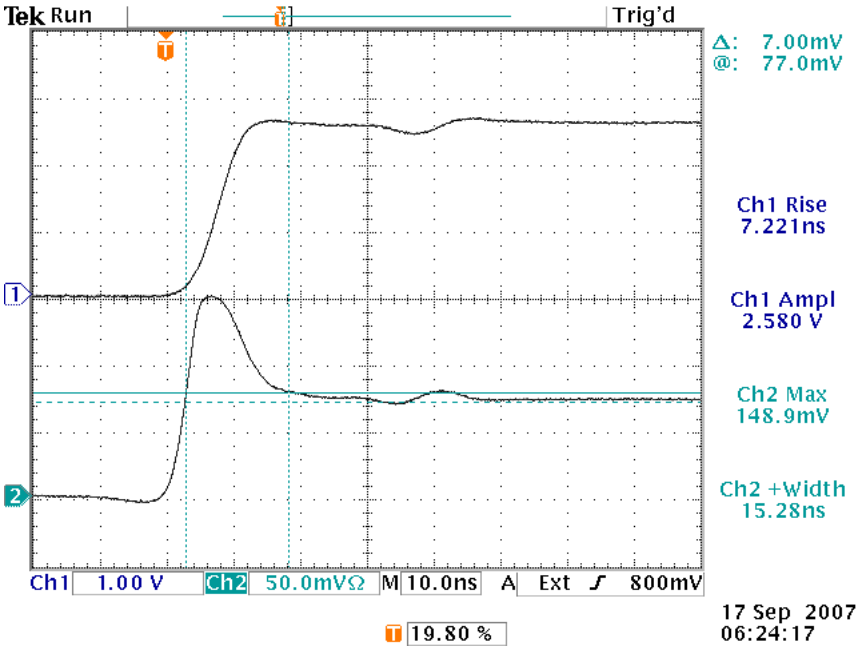
Real results illustrating this calculation are given in the “TYPICAL RESULTS – SOT23 DEVICES” section later in this manual.

TYPICAL RESULTS – SINGLE DEVICES

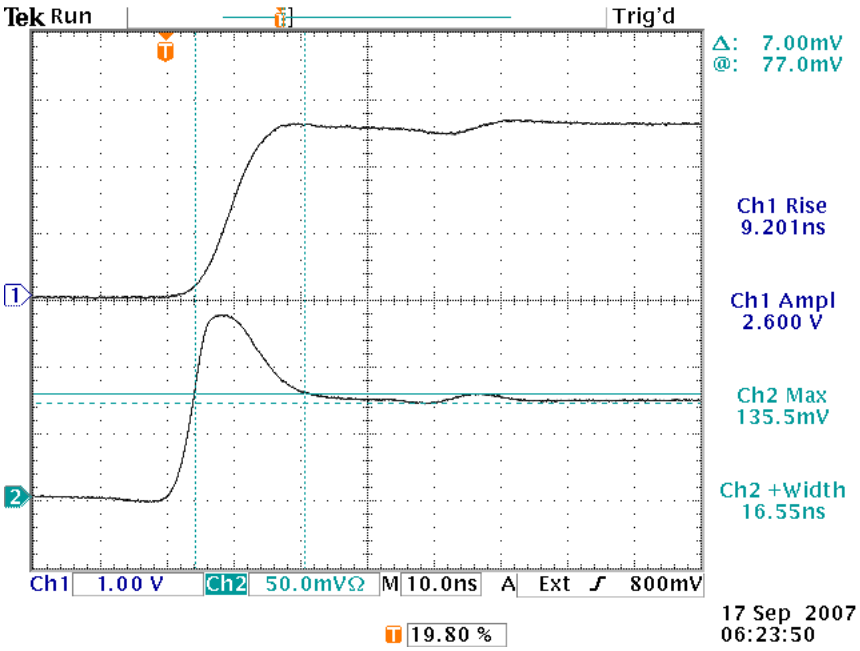
Obtaining meaningful results with the AVR-EBF6-B requires care, experience, and an understanding of diode transient behavior and the impact of inductive and capacitive parasitics. To assist the user, typical results are provided below. The user should be able to reliably duplicate these results.

1N5811 RESULTS

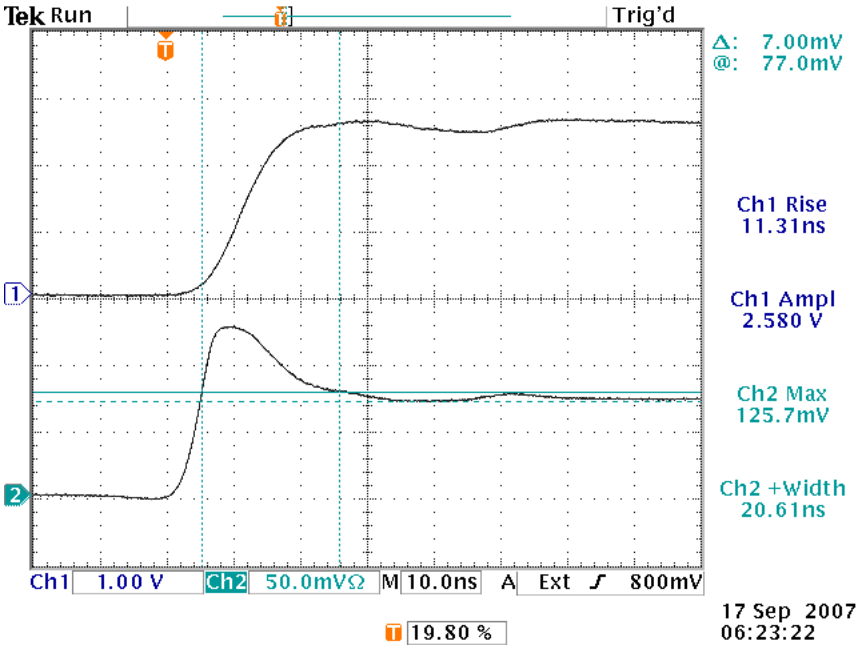
A customer-supplied 1N5811 engineering sample (sample #51) was tested in the AVX-TRF-ANB jig, using the 8 ns, 10 ns, and 12 ns rise time filters, with the amplitude set to +25.7V (such that the forward current I_F = 500 mA). The following forward recovery waveforms were obtained from the test jig outputs:



Top – Test jig MON output (V_{IN}/10, +25.7V, with ~ 8 ns rise time). 1 V/div, 10 ns/div.
Bottom – Test jig main output (V_{DUT}/10). 50 mV/div, 10 ns/div.



Top – Test jig MON output (V_{IN}/10, +25.7V, with ~ 10 ns rise time). 1 V/div, 10 ns/div.
Bottom – Test jig main output (V_{DUT}/10). 50 mV/div, 10 ns/div.



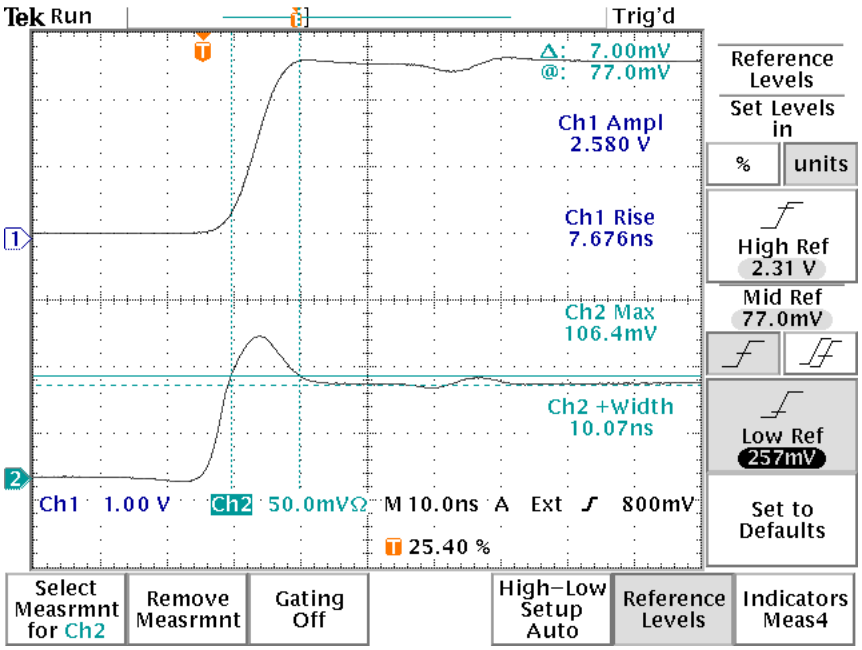
Top – Test jig MON output (V_{IN}/10, +25.7V, with ~ 12 ns rise time). 1 V/div, 10 ns/div.
Bottom – Test jig main output (V_{DUT}/10). 50 mV/div, 10 ns/div.

The results are summarized in the following table:

Filter Used	V_{FM}	V_F	t_{FR}
8 ns	1.489 V	0.70 V	15.28 ns
10 ns	1.355 V	0.70 V	16.55 ns
12 ns	1.257 V	0.70 V	20.61 ns

MQ1N5811US RESULTS

The Microsemi MQ1N5811US was tested with the amplitude set to +25.7V (such that the forward current I_F = 500 mA), using an 8 ns rise time filter and the AVX-TFR-MELF test jig. The following forward recovery waveform was obtained at the test jig "OUT" terminal:



Top – Test jig MON output (V_{IN}/10, +25.7V, with ~ 8 ns rise time). 1 V/div, 10 ns/div.
Bottom – Test jig main output (V_{DUT}/10). 50 mV/div, 10 ns/div.

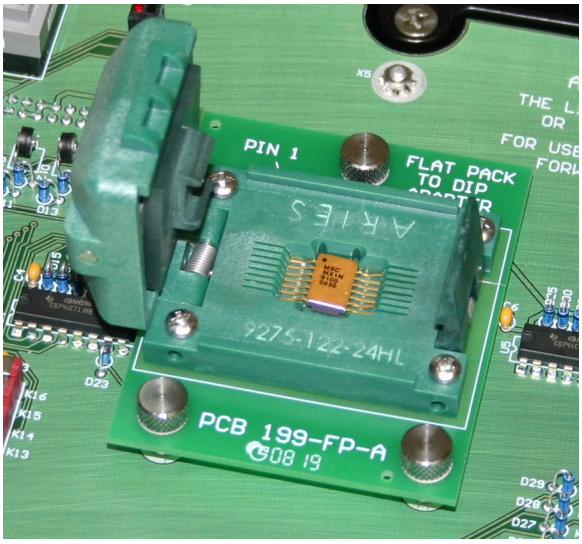
Under these conditions, V_{FM} = 1.064V, V_F = 0.70V, and t_{FR} = 10.07 ns (measured at 1.1×V_F).

TYPICAL RESULTS – DIPS AND FLAT-PACKS

The results in this section are typical of units with the -DIPFP option.

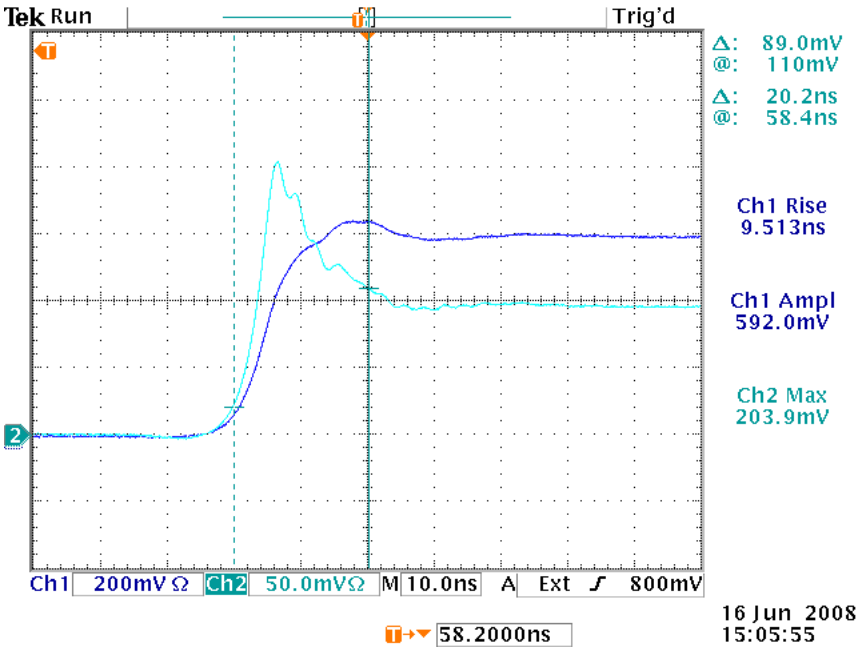
1N6100 FLAT-PACK

A 1N6100 14-pin flat-pack device was installed in the AVX-TFR-DIPFP test jig, using the DIP-to-flat-pack adapter.



Installed 1N6100 DUT, before closing clamshell and lid

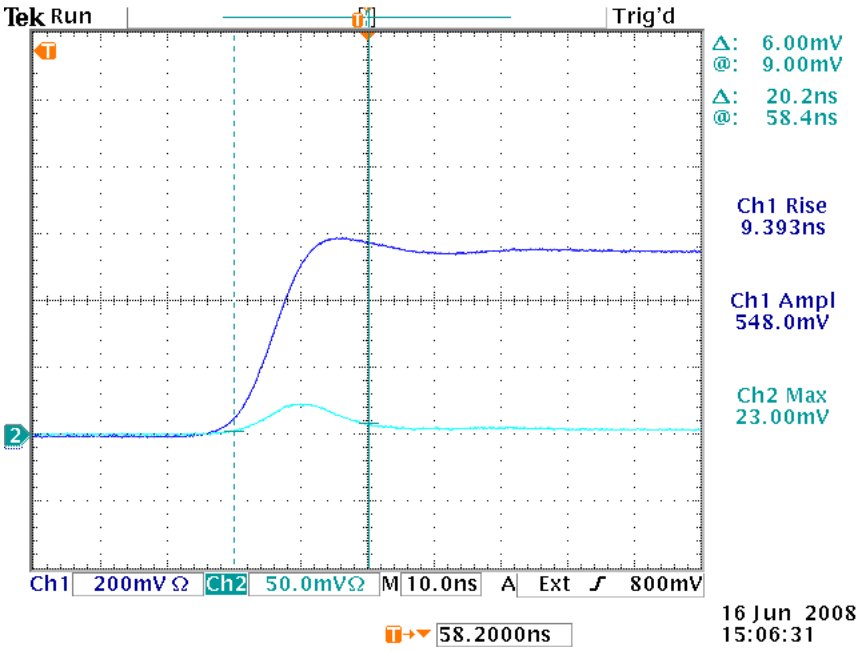
With the amplitude set at +5.9V, to generate a forward current of 100 mA ((5.9V – 0.9V) / 50 Ohms = 100 mA), and a 10 ns rise time filter, and ANODE = pin socket 16 (corresponding to device pin 14), and CATHODE = pin socket 1, the following waveforms were generated on the jig's two outputs:



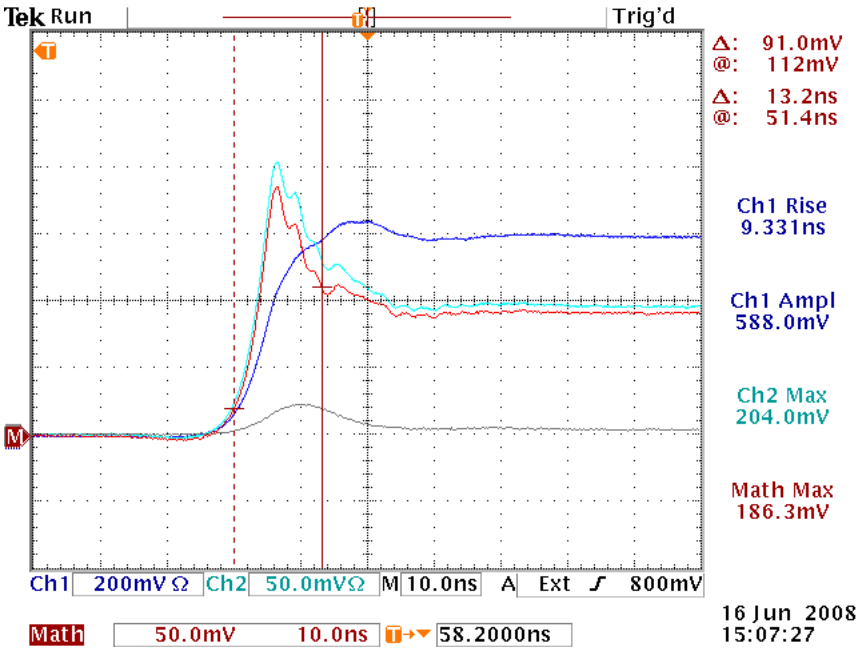
Dark blue: MON output (V_{IN}/10, +5.9V, with ~ 10 ns rise time). 0.2 V/div, 10 ns/div.
Light blue: Main output (V_{DUT}/10). 50 mV/div, 10 ns/div.

The MIL-PRF-19500/474F "slash sheet" for the 1N6100 specifies a maximum forward voltage of 5V and a maximum forward recovery time of 15 ns for recovery to 1.1 Volts. The peak V_{DUT} of 2.039 V easily meets this voltage requirement. Unfortunately, these waveforms show a t_{FR} = 20.2 ns time between the 10% point of V_{MON} and the point where V_{DUT} = 1.1V.

However, part of the output waveform is due to the parasitic inductance of the grounding relay. Leaving all settings unchanged except than ANODE = CATHODE = pin socket 1, this waveform is obtained:



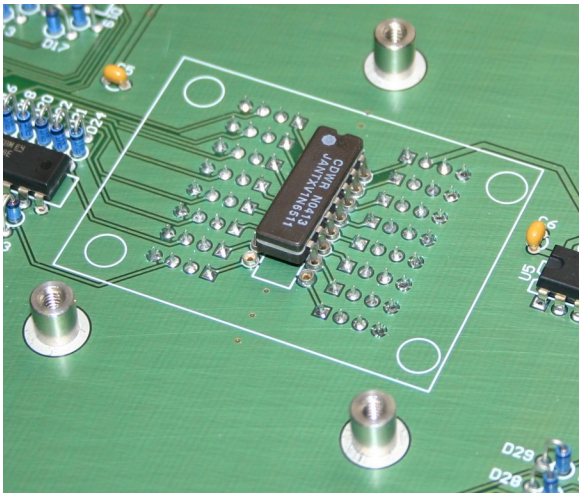
This shows an output "bump" of 230 mV in magnitude, due solely to the grounding relay inductance. Now, we save this "bump" waveform, and subtract it from the original DUT waveform (generated with ANODE = pin socket 16 and CATHODE = pin socket 1):



In this plot, the red waveform is the calculated "true" diode V_F, with the small effect of the grounding relay inductance subtracted out. With this correction, the new measured t_{FR} is 13.2 ns, within the expected limit.

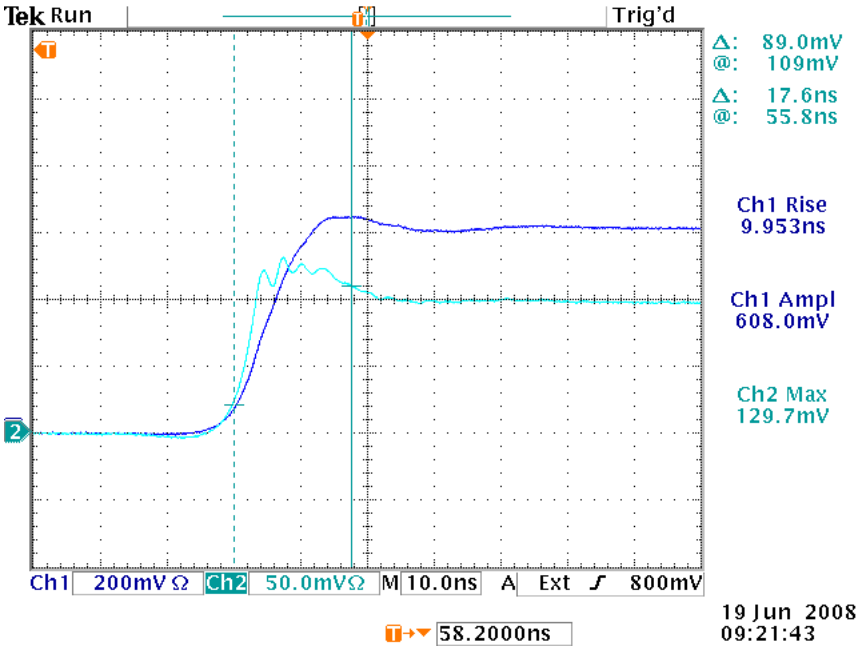
1N6511 DIP

A 1N6511 14-pin DIP device was installed in the AVX-TFR-DIPFP test jig:



Installed 1N6511 DUT, before closing the lid

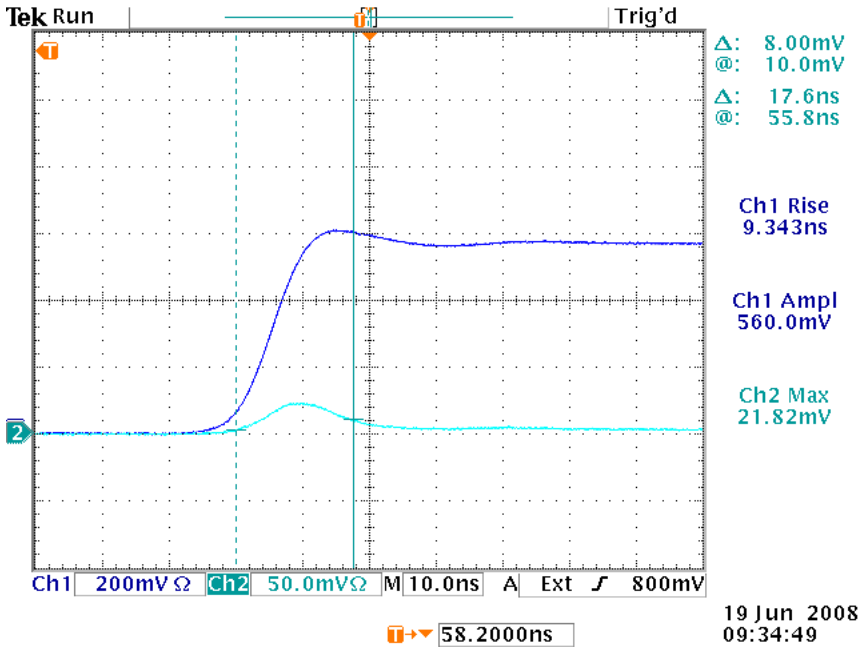
With the amplitude set at +6.0V, to generate a forward current of 100 mA ((6V – 1V) / 50 Ohms = 100 mA), and a 10 ns rise time filter, and ANODE = pin socket 16 (corresponding to device pin 14), and CATHODE = pin socket 1, the following waveforms were generated on the jig's two outputs:



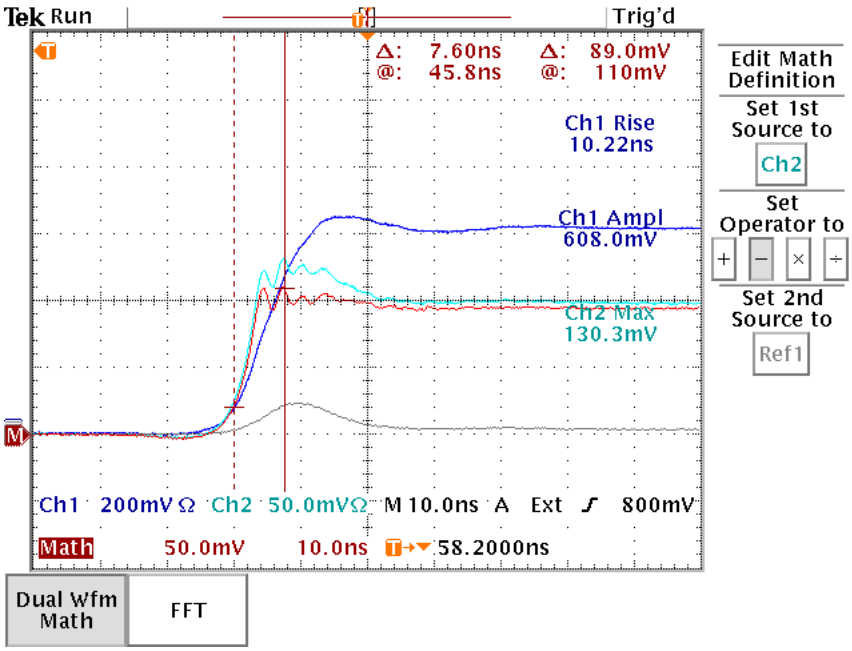
Dark blue: MON output (V_{IN}/10, +6V, with ~ 10 ns rise time). 0.2 V/div, 10 ns/div.
Light blue: Main output (V_{DUT}/10). 50 mV/div, 10 ns/div.

The MIL-PRF-19500/474F “slash sheet” for the 1N6511 specifies a maximum forward voltage of 5V and a maximum forward recovery time of 15 ns for recovery to 1.1 Volts. The peak V_{DUT} of 1.297 V easily meets this voltage requirement. Unfortunately, these waveforms show a t_{FR} = 17.6 ns time between the 10% point of V_{MON} and the point where V_{DUT} = 1.1V.

However, part of the output waveform is due to the parasitic inductance of the grounding relay. Leaving all settings unchanged except than ANODE = CATHODE = pin socket 1, this waveform is obtained:



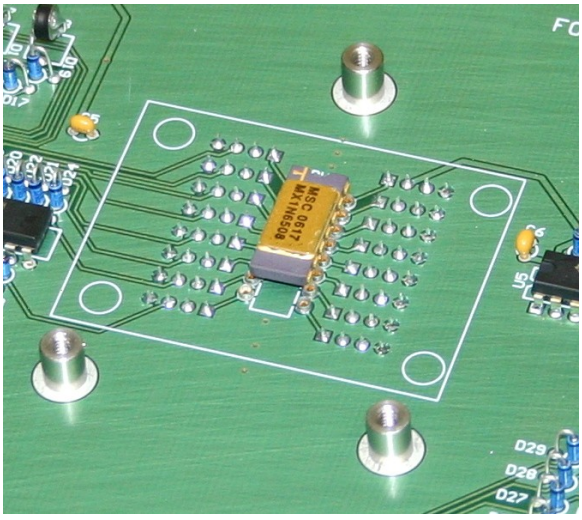
This shows an output “bump” of 218 mV in magnitude, due solely to the grounding relay inductance. Now, we save this “bump” waveform, and subtract it from the original DUT waveform (generated with ANODE = pin socket 16 and CATHODE = pin socket 1):



In this plot, the red waveform is the calculated "true" diode V_F, with the small effect of the grounding relay inductance subtracted out. With this correction, the new measured t_{FR} is 7.6 ns, within the expected limit.

1N6508 DIP

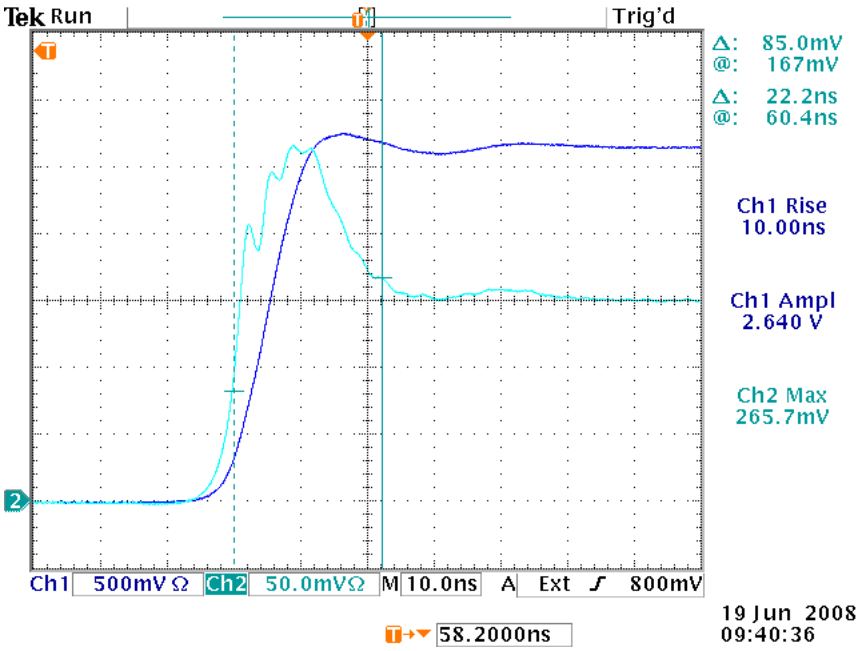
A 1N6508 14-pin DIP device was installed in the AVX-TFR-DIPFP test jig:



Installed 1N6508 DUT, before closing the lid

With the amplitude set at +26.5V, to generate a forward current of 500 mA ((26.5V – 1.5V) / 50 Ohms = 100 mA), and a 10 ns rise time filter, and ANODE = pin socket 2,

and CATHODE = pin socket 1, the following waveforms were generated on the jig's two outputs:



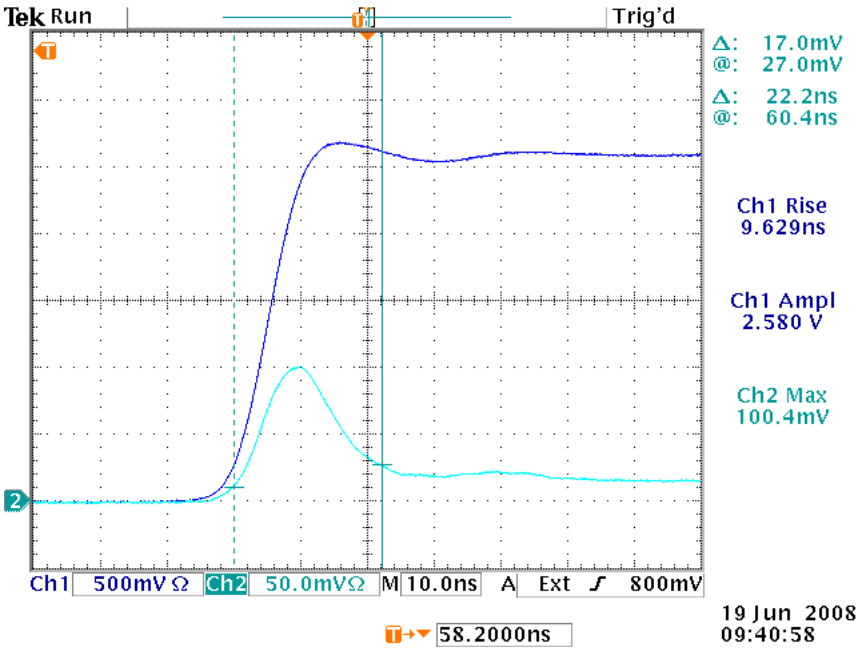
Dark blue: MON output (V_{IN}/10, +26.5V, with ~ 10 ns rise time). 0.5 V/div, 10 ns/div.
Light blue: Main output (V_{DUT}/10). 50 mV/div, 10 ns/div.

The MIL-PRF-19500/474F “slash sheet” for the 1N6508 specifies a maximum forward voltage of 5V and a maximum forward recovery time of 40 ns for recovery to 1.1 Volts. The peak V_{DUT} of 2.66 V easily meets this voltage requirement.

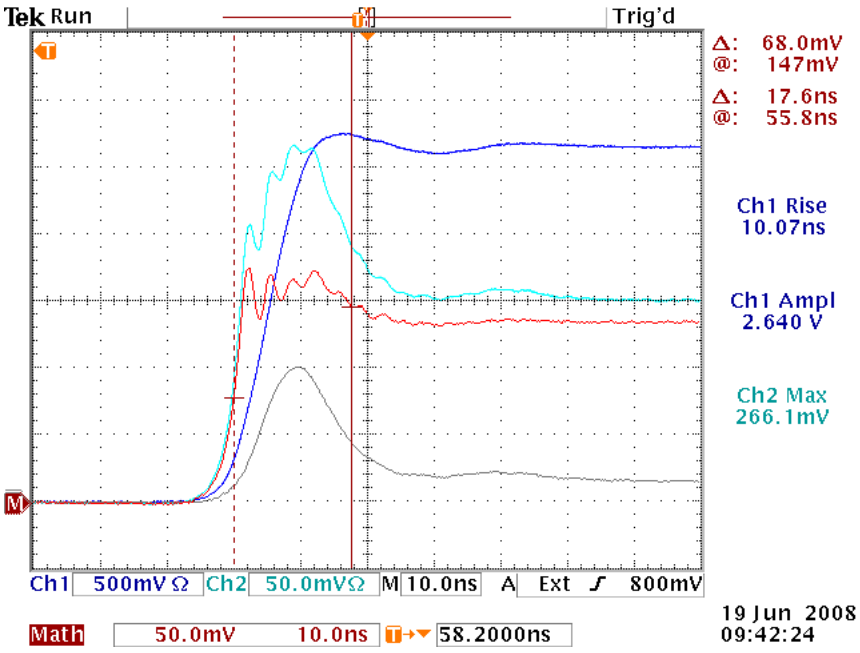
However, the forward voltage does not recover to 1.1V DC, as called for in the slash sheet. However, the slash sheet also specifies a maximum steady-state forward voltage drop of 1.5V at 500 mA, so it is strange that it specifies “V_{fr} = 1.1 V dc” for the forward recovery test. For this test, we'll ignore that and use the point 10% above the steady voltage.

These waveforms show a t_{FR} = 22.2 ns time between the 10% point of V_{MON} and the point 10% above the steady voltage.

However, part of the output waveform is due to the parasitic inductance of the grounding relay. Leaving all settings unchanged except than ANODE = CATHODE = pin socket 1, this waveform is obtained:



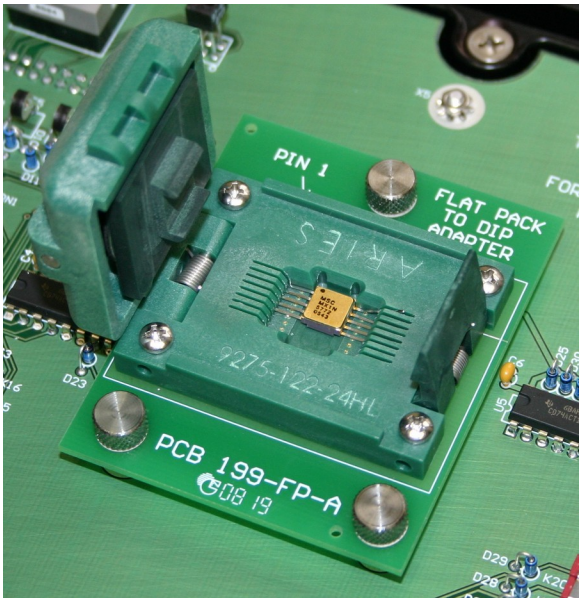
This shows an output "bump" of 1.0V in magnitude, due solely to the grounding relay inductance. Now, we save this "bump" waveform, and subtract it from the original DUT waveform (generated with ANODE = pin socket 2 and CATHODE = pin socket 1):



In this plot, the red waveform is the calculated "true" diode V_F, with the small effect of the grounding relay inductance subtracted out. With this correction, the new measured t_{FR} is 17.6 ns, within the expected limit.

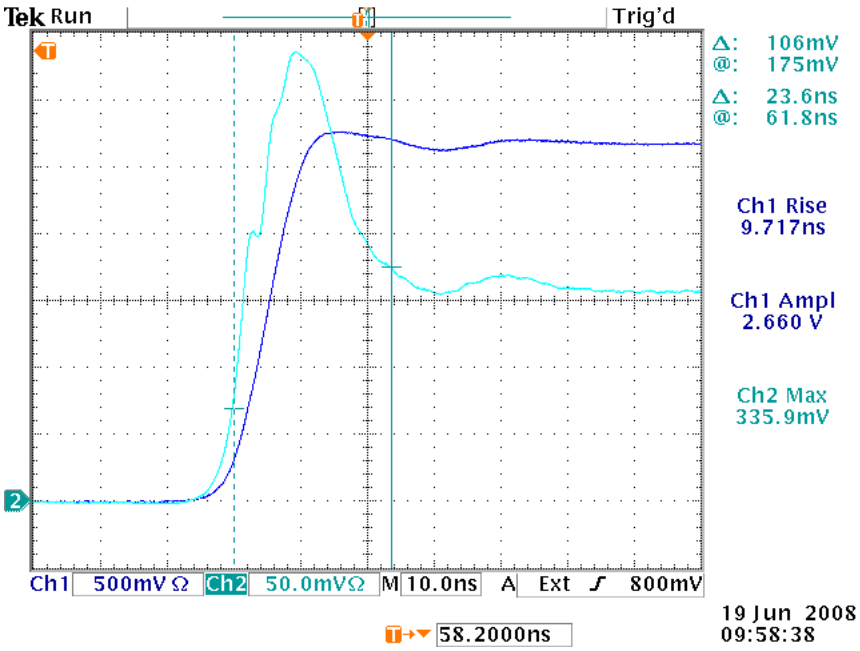
1N5772 FLAT-PACK

A 1N5772 10-pin flat-pack device was installed in the AVX-TFR-DIPFP test jig, using the DIP-to-flat-pack adapter.



Installed 1N5772 DUT, before closing clamshell and lid

With the amplitude set at +26.5V, to generate a forward current of 500 mA ((26.5V – 1.5V) / 50 Ohms = 100 mA), and a 10 ns rise time filter, and ANODE = pin socket 1, and CATHODE = pin socket 5, the following waveforms were generated on the jig's two outputs:



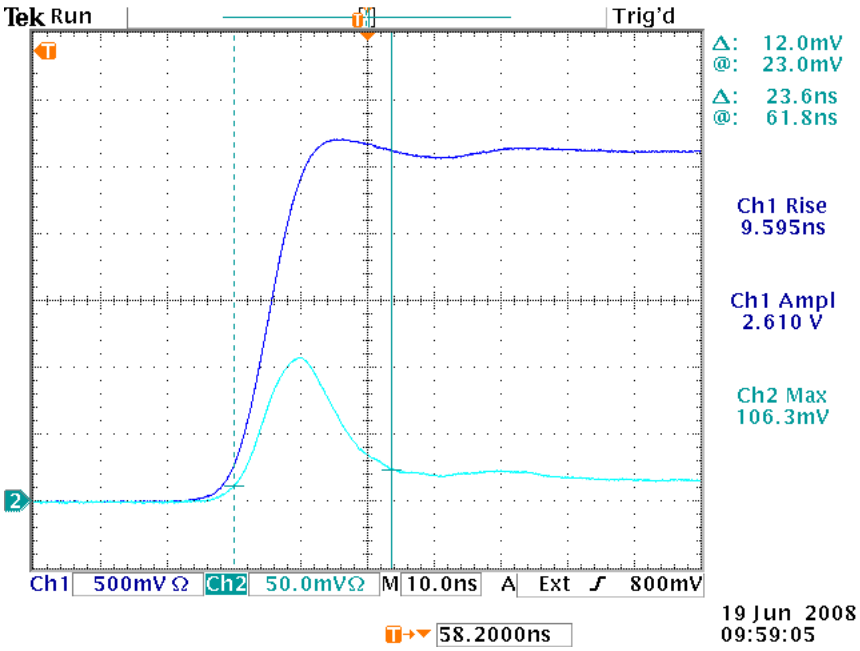
Dark blue: MON output (V_{IN}/10, +26.5V, with ~ 10 ns rise time). 0.5 V/div, 10 ns/div.
Light blue: Main output (V_{DUT}/10). 50 mV/div, 10 ns/div.

The MIL-PRF-19500/474F "slash sheet" for the 1N5772 specifies a maximum forward voltage of 5V and a maximum forward recovery time of 40 ns for recovery to 1.1 Volts. The peak V_{DUT} of 3.36 V easily meets this voltage requirement.

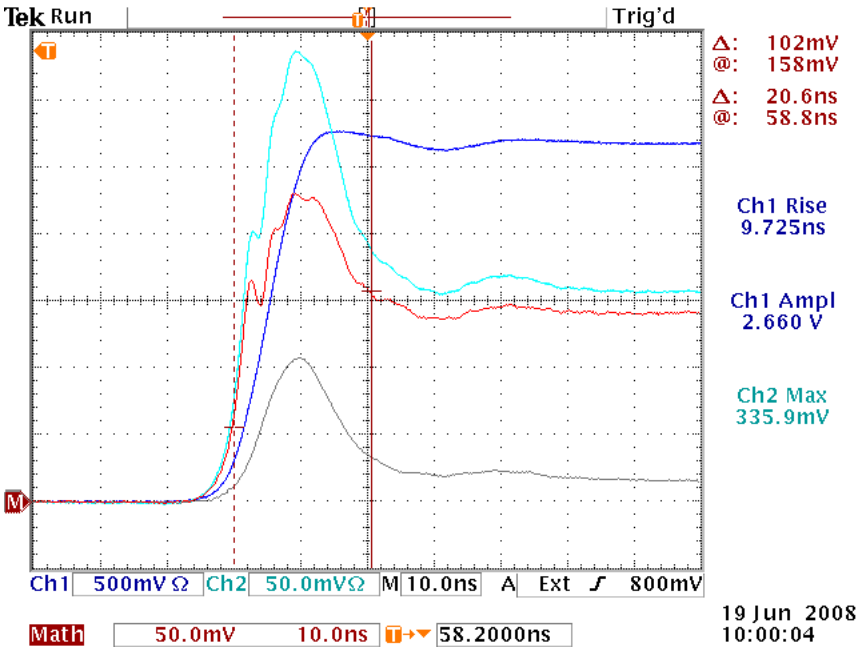
However, the forward voltage does not recover to 1.1V DC, as called for in the slash sheet. However, the slash sheet also specifies a maximum steady-state forward voltage drop of 1.5V at 500 mA, so it is strange that it specifies "V_{fr} = 1.1 V dc" for the forward recovery test. For this test, we'll ignore that and use the point 10% above the steady voltage.

These waveforms show a t_{FR} = 23.6 ns time between the 10% point of V_{MON} and the point 10% above the steady voltage.

However, part of the output waveform is due to the parasitic inductance of the grounding relay. Leaving all settings unchanged except than ANODE = CATHODE = pin socket 5, this waveform is obtained:



This shows an output "bump" of 1.06V in magnitude, due solely to the grounding relay inductance. Now, we save this "bump" waveform, and subtract it from the original DUT waveform (generated with ANODE = pin socket 1 and CATHODE = pin socket 5):



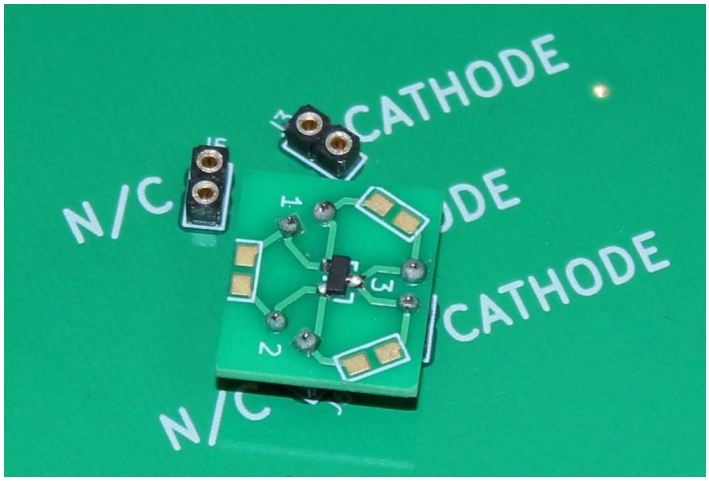
In this plot, the red waveform is the calculated "true" diode V_F, with the small effect of the grounding relay inductance subtracted out. With this correction, the new measured t_{FR} is 20.6 ns, within the expected limits.

TYPICAL RESULTS – SOT23 DEVICES

The results in this section are typical of units with the -SOT23B option.

MMBD4148CC

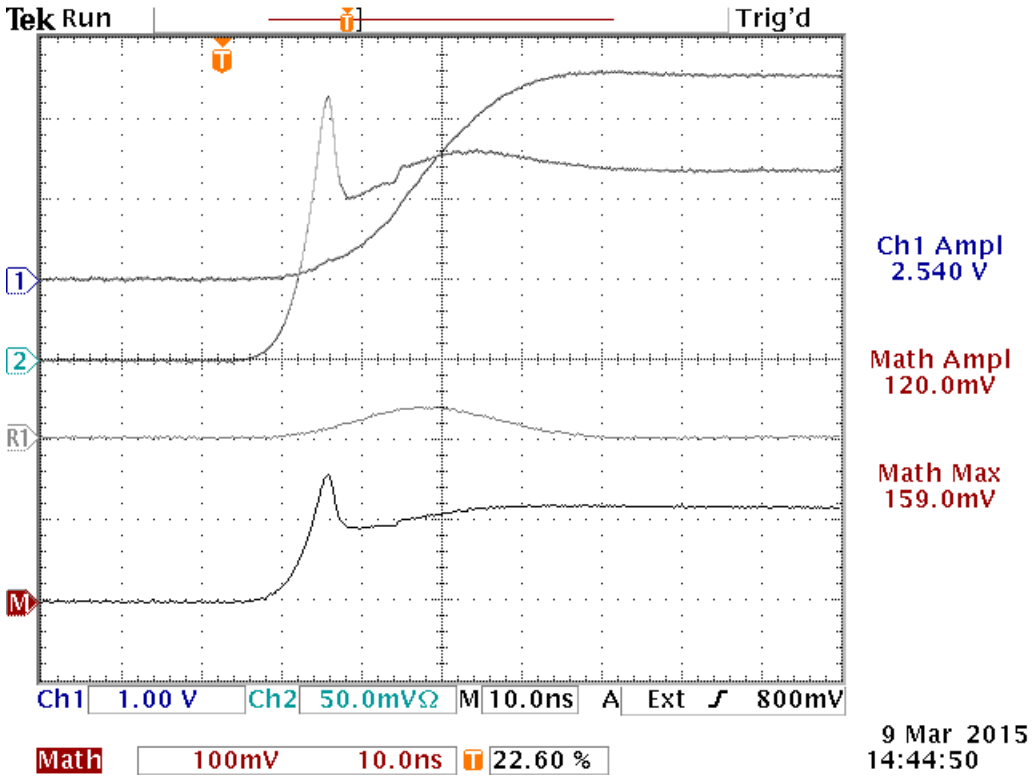
A Fairchild MMBD4148CC SMT device was installed in the AVX-TFR-SOT23B test jig, as shown below. Pin 1 is the anode, and pin 3 is the cathode.



With the amplitude set at ~25V, to generate a forward current of 500 mA, and a 20 ns rise time filter, the waveforms “1” and “2” in the photo below were generated on the jig's two outputs.

Waveform “R1” shows the main output if the MMBD4148CC is replaced with a zero Ohm jumper. This establishes the effect of the jig and daughterboard parasitic inductance.

Waveform “M” shows “2” - “R1” - that is, the DUT waveform with the effect of the parasitic inductance removed. This shows that the narrow spike is the true forward transient, and it is extremely short.



"1" waveform: MON output (V_{IN}/10, +25V, with ~20 ns rise time). 1 V/div, 10 ns/div.

"2" waveform: Main output (V_{DUT}/10). 50 mV/div, 10 ns/div.

"R1" waveform: Show the main output when the MMBD4148CC is replaced with a 0Ω jumper, to establish the effect of the jig/daughterboard parasitic inductance.

"M" waveform: Shows "2" - "R1" - that is, the DUT waveform with the effect of the parasitic inductance removed. This shows that the narrow spike is the true forward transient, and it is extremely short.

TROUBLESHOOTING

If you obtain “strange” output waveforms, or unexpected values of t_{RR}, keep these points in mind:

1) The test jig output *must* be terminated with 50 Ohms.

2) Keep device lead lengths as short as possible, to minimize parasitic inductance.

3) The test jig lid must be closed, or the pulser output will be disabled.

For technical support, contact info@avtechpulse.com. Sample waveforms and digital photos of your setup are always helpful!

AVX-TFR-DIPFP JIG RELAYS

The AVX-TFR-DIPFP test jig is particularly complex, because it uses 32 internal coaxial cables and 48 relays to switch the input, output, and ground signals to the 16 pin sockets.

If you suspect that one or more of the pins sockets is not operating correctly, follow this procedure to test the various internal connections:

1) Remove the flat-pack-to-DIP adapter from the AVX-TFR-DIPFP test jig, if present.

2) Connect the AVX-TFR-DIPFP test jig to the mainframe using only the DB-25 control cable. Leave all external coaxial cables disconnected.

3) Turn the mainframe on. Confirm that the Cathode setting is “1”. Measure the resistance between pin socket 1 and ground. It should be < 1 Ω. (The shield of the SMA connectors below the hinge can be used as grounds, or screws securing the hinges to the chassis. The threaded standoffs that accept the flat-pack-to-DIP adapter are *not* grounded.)

4) Use the front-panel menus to change the “Cathode” setting to “2”. The resistance between pin 1 and ground should be > 10 kΩ, and the resistance between pin 2 and ground should be < 1 Ω. Repeat for pins 3-16.

5) Confirm that the Anode setting is “1”. Measure the resistance between pin socket 1 and the center conductor on the “IN” SMA connector (located below the jig hinge). It should be 50 Ω.

6) Use the front-panel menus to change the “Anode” setting to “2”. The resistance between pin 1 and “IN” should become > 10 kΩ. The resistance between pin 2

and “IN” should be 50 Ω. Repeat for pins 3-16.

7) Confirm that the Anode setting is “1”. Measure the resistance between pin socket 1 and the center conductor on the “OUT” SMA connector (located below the jig hinge). It should be 450 Ω.

8) Use the front-panel menus to change the “Anode” setting to “2”. The resistance between pin 1 and “OUT” should become > 10 kΩ. The resistance between pin 2 and “OUT” should be 450 Ω. Repeat for pins 3-16.

9) Measure the resistance between the center conductor on the “IN” SMA and the center conductor on the “MON” SMA . It should be 450 Ω.

If the measurements do not agree with the expected values, contact the Avtech factory (info@avtechpulse.com).

PROGRAMMING YOUR PULSE GENERATOR

KEY PROGRAMMING COMMANDS

The “Programming Manual for -B Instruments” describes in detail how to connect the pulse generator to your computer, and the programming commands themselves. A large number of commands are available; however, normally you will only need a few of these. Here is a basic sample sequence of commands that might be sent to the instrument after power-up:

*rst	(resets the instrument)
trigger:source internal	(selects internal triggering)
frequency 1000 Hz	(sets the frequency to 1000 Hz)
pulse:delay 1 us	(sets the delay to 1 us)
pulse:width 10 us	(sets the positive pulse width to 10 us)
volt:ampl +25.7	(sets the positive pulse amplitude to +25.7 V)
output on	(turns on the output)

For triggering a single event, this sequence would be more appropriate:

*rst	(resets the instrument)
trigger:source hold	(turns off all triggering)
output on	(turns on the output)
pulse:delay 1 us	(sets the delay to 1 us)
pulse:width 10 us	(sets the positive pulse width to 10 us)
volt:ampl +25.7	(sets the positive pulse amplitude to +25.7 V)
trigger:source immediate	(generates a single non-repetitive trigger event)
trigger:source hold	(turns off all triggering)
output off	(turns off the output)

To set the instrument to trigger from an external TTL signal applied to the rear-panel TRIg connector, use:

*rst	(resets the instrument)
trigger:source external	(selects internal triggering)
pulse:delay 1 us	(sets the delay to 1 us)
pulse:width 10 us	(sets the positive pulse width to 10 us)
volt:ampl +25.7	(sets the positive pulse amplitude to +25.7 V)
output on	(turns on the output)

These commands will satisfy 90% of your programming needs.

ALL PROGRAMMING COMMANDS

For more advanced programmers, a complete list of the available commands is given below. These commands are described in detail in the “Programming Manual for -B Instruments”. (Note: this manual also includes some commands that are not implemented in this instrument. They can be ignored.)

Keyword	Parameter	Notes
LOCAL		
OUTPut:		
:[STATe]	<boolean value>	
:PROTection		
:TRIPped?		[query only]
REMOTE		
[SOURce]:		
:FREQuency		
[:CW | FIXed]	<numeric value>	
[SOURce]:		
:PULSe		
:PERiod	<numeric value>	
:WIDTh	<numeric value>	
:DELay	<numeric value>	
:GATE		
:LEVel	HIgh | LOw	
[SOURce]:		
:VOLTage		
[:LEVel]		
[:IMMediate]		
[:AMPLitude]	<numeric value>	
:PROTection		
:TRIPped?		[query only]
STATUS:		
:OPERation		
:[EVENt]?		[query only, always returns "0"]
:CONDition?		[query only, always returns "0"]
:ENABle	<numeric value>	[implemented but not useful]
:QUEStionable		
:[EVENt]?		[query only, always returns "0"]
:CONDition?		[query only, always returns "0"]
:ENABle	<numeric value>	[implemented but not useful]
SYSTem:		
:COMMunicate		
:GPIB		
:ADDRess	<numeric value>	
:SERial		
:CONTrol		
:RTS	ON | IBFull | RFR	
:[RECeive]		
:BAUD	1200 | 2400 | 4800 | 9600	
:BITS	7 | 8	
:ECHO	<boolean value>	
:PARity		
:[TYPE]	EVEN | ODD | NONE	
:SBITS	1 | 2	
:ERRor		

:[NEXT]?		[query only]
:COUNT?		[query only]
:VERSion?		[query only]
TRIGger:		
:SOURce	INTernal | EXTernal | MANual | HOLD | IMMediate	
*CLS		[no query form]
*ESE	<numeric value>	
*ESR?		[query only]
*IDN?		[query only]
*OPC		
*SAV	0 | 1 | 2 | 3	[no query form]
*RCL	0 | 1 | 2 | 3	[no query form]
*RST		[no query form]
*SRE	<numeric value>	
*STB?		[query only]
*TST?		[query only]
*WAI		[no query form]

MECHANICAL INFORMATION

TOP COVER REMOVAL

If necessary, the interior of the instrument may be accessed by removing the four Phillips screws on the top panel. With the four screws removed, the top cover may be slid back (and off).

⚠ Always disconnect the power cord and allow the instrument to sit unpowered for 10 minutes before opening the instrument. This will allow any internal stored charge to discharge.

There are no user-adjustable internal circuits. For repairs other than fuse replacement, please contact Avtech (info@avtechpulse.com) to arrange for the instrument to be returned to the factory for repair. Service is to be performed solely by qualified service personnel.

⚠ Caution: High voltages are present inside the instrument during normal operation. Do not operate the instrument with the cover removed.

RACK MOUNTING

A rack mounting kit is available. The -R5 rack mount kit may be installed after first removing the one Phillips screw on the side panel adjacent to the front handle.

ELECTROMAGNETIC INTERFERENCE

To prevent electromagnetic interference with other equipment, all used outputs should be connected to shielded loads using shielded coaxial cables. Unused outputs should be terminated with shielded coaxial terminators or with shielded coaxial dust caps, to prevent unintentional electromagnetic radiation. All cords and cables should be less than 3m in length.

MAINTENANCE

REGULAR MAINTENANCE

This instrument does not require any regular maintenance.

On occasion, one or more of the four rear-panel fuses may require replacement. All fuses can be accessed from the rear panel. See the “FUSES” section for details.

CLEANING

If desired, the interior of the instrument may be cleaned using compressed air to dislodge any accumulated dust. (See the “TOP COVER REMOVAL” section for instructions on accessing the interior.) No other cleaning is recommended.

TRIGGER DAMAGE

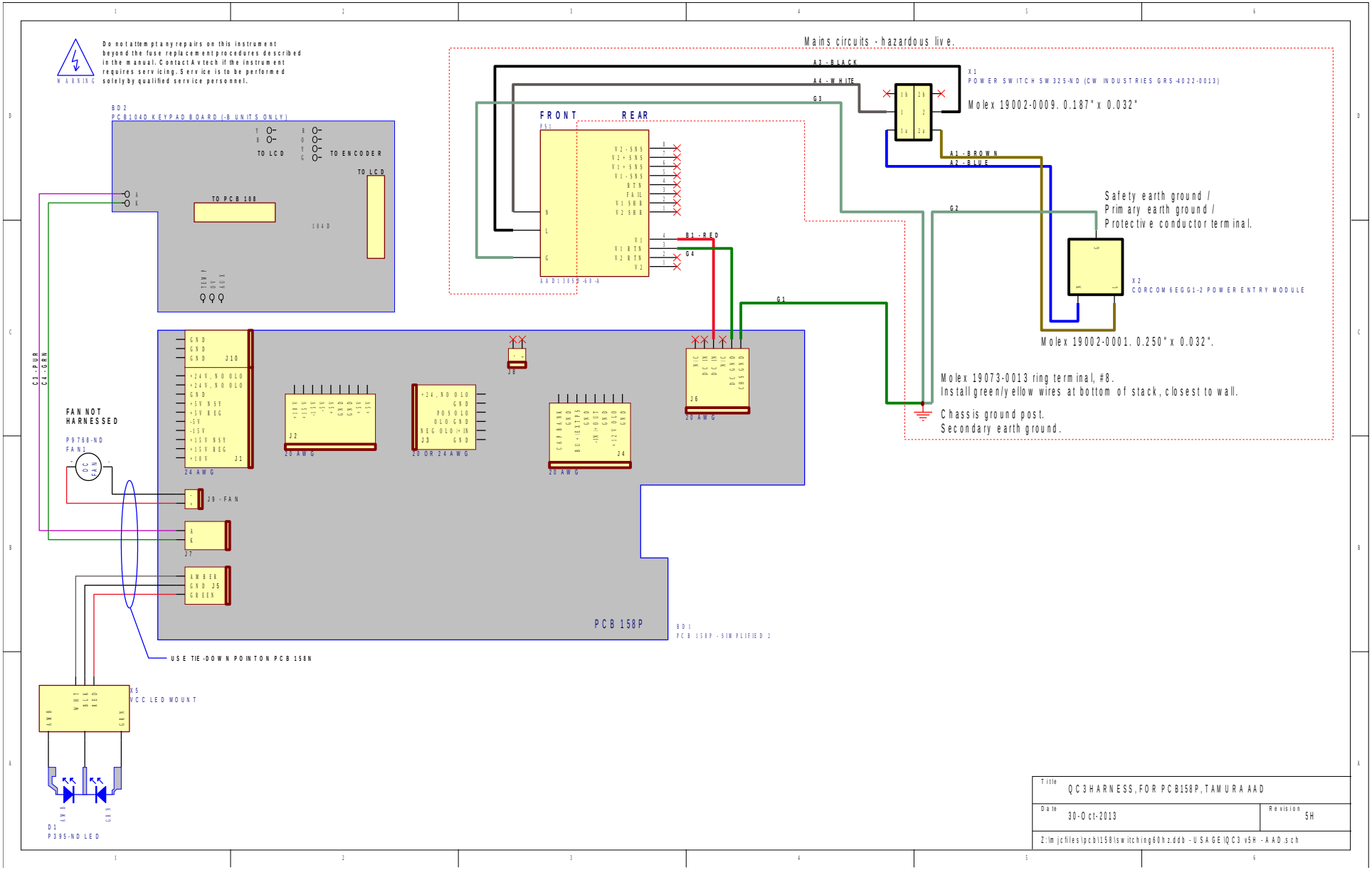
The rear-panel TRIG input, used in the external trigger mode, is protected by a diode clamping circuit. However, the protection circuit is not foolproof, and it is possible for a grossly excessive signal to damage the trigger circuitry on the main timing control board (the 4×10 inch board on the right side of the instrument).

The IC that is most likely to fail under these conditions is installed in a socket. It is a standard TTL IC in a 16-pin plastic DIP package, model 74F151 or equivalent.

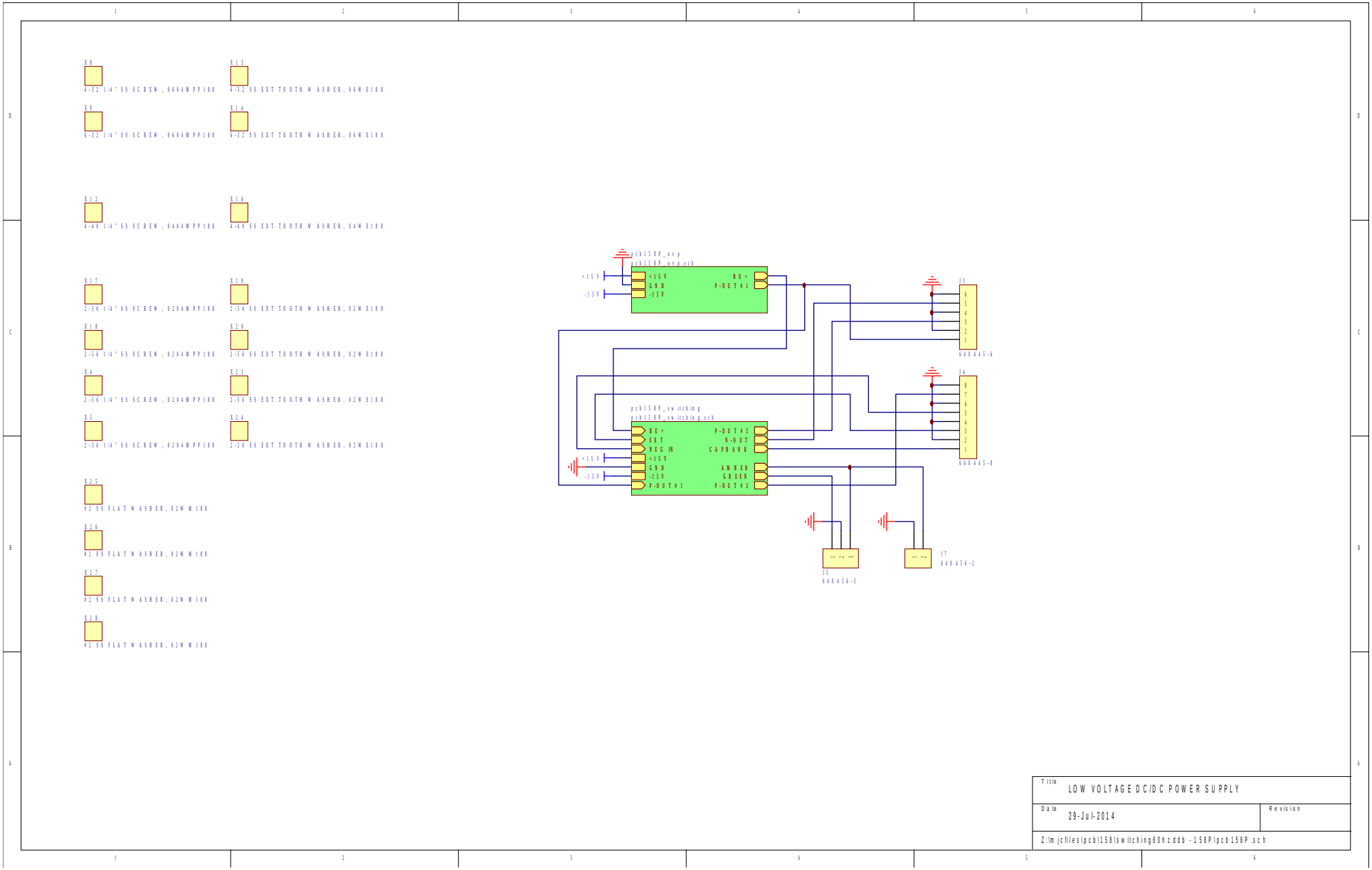
If you suspect that this IC has been damaged, turn off the power and replace this IC. It may be replaced by a 74F151, 74LS151, 74ALS151, or 74HCT151.

WIRING DIAGRAMS

WIRING OF AC POWER

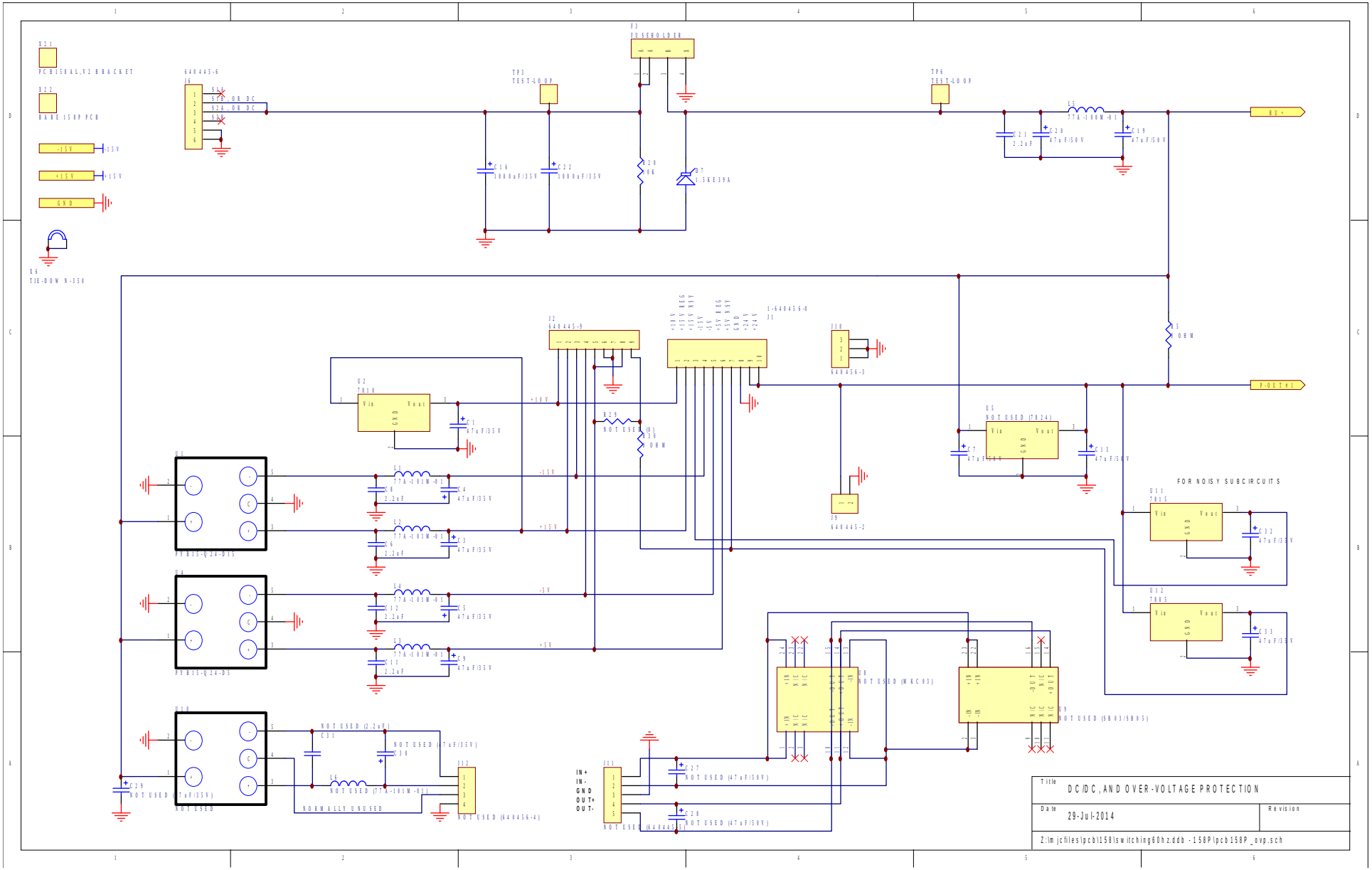


PCB 158P - LOW VOLTAGE POWER SUPPLY, 1/3

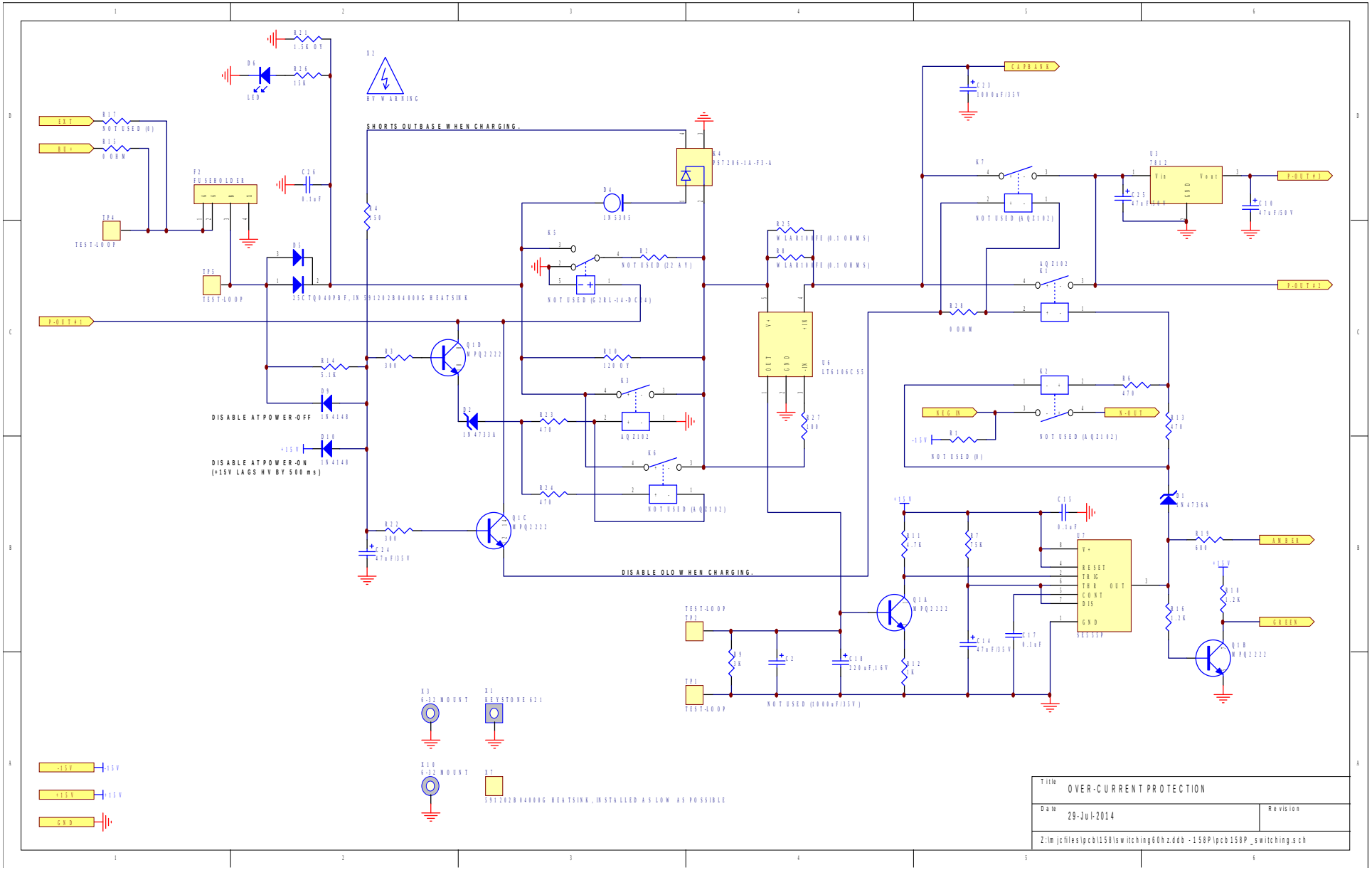


Title	LOW VOLTAGE DC/DC POWER SUPPLY
Date	29-Jul-2014
Revision	
Z:\mjcfiles\pcb\158\switching60hz.ddb - 158P\pcb158P.sch	

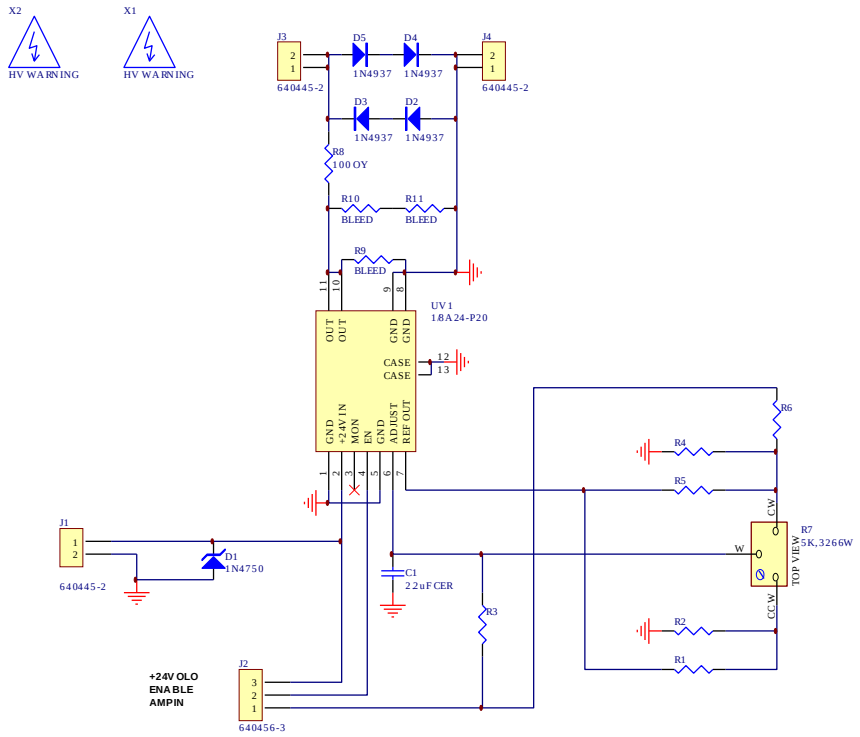
PCB 158P - LOW VOLTAGE POWER SUPPLY, 2/3



PCB 158P - LOW VOLTAGE POWER SUPPLY, 3/3

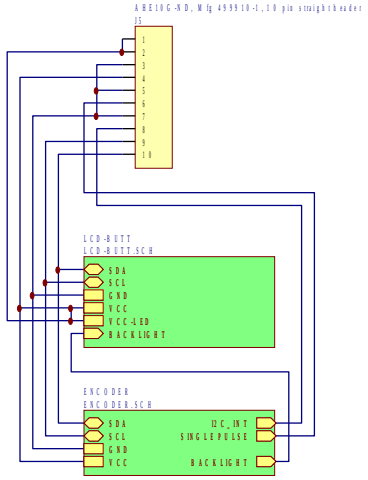


PCB 168B - HIGH VOLTAGE DC POWER SUPPLY



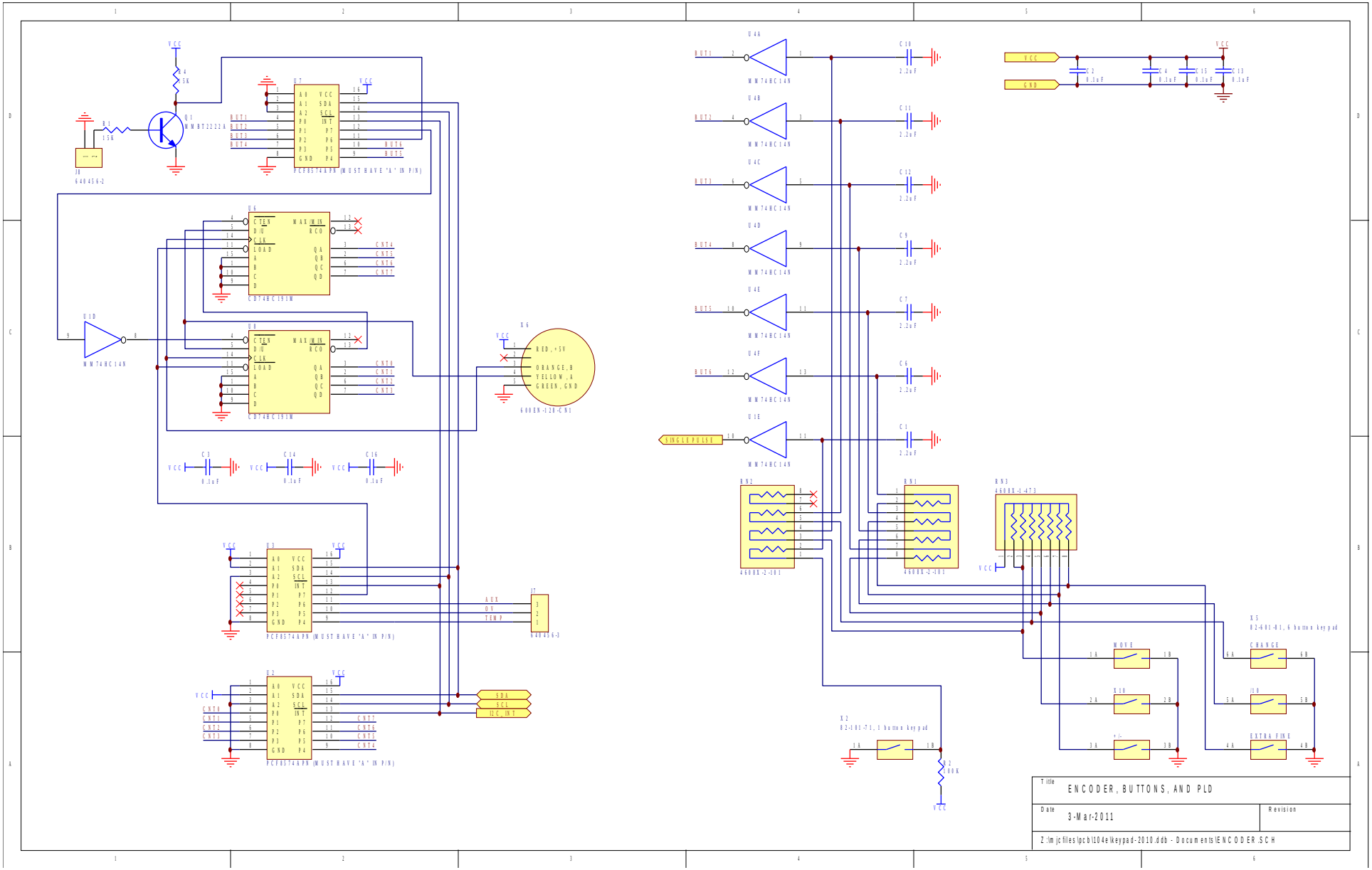
Title	UV-A CONTROL PCB
Date	3-Nov-2005
Revision	1
Z:\mjcfiles\pcb\168\UV-A control\UV-A control.ddb - 168B\PCB168B.sch	

PCB 104E - KEYPAD / DISPLAY BOARD, 1/3

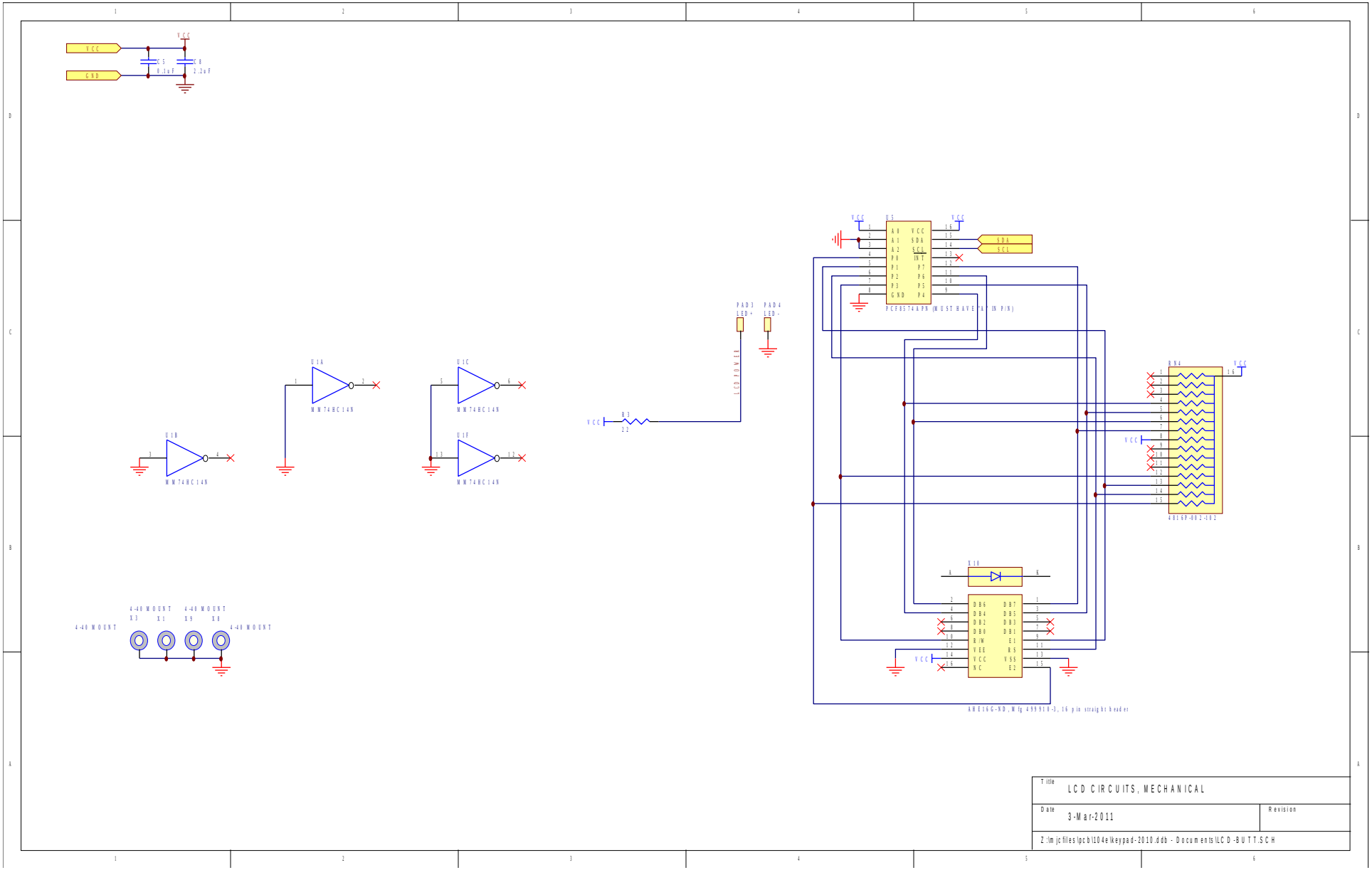


Title	PANEL TOP-LEVEL SCHEMATIC
Date	3-Mar-2011
Revision	
Z:\mjcfiles\pcb\104e\keypad-2010.ddb - Documents\Panelbrd.prj	

PCB 104E - KEYPAD / DISPLAY BOARD, 2/3

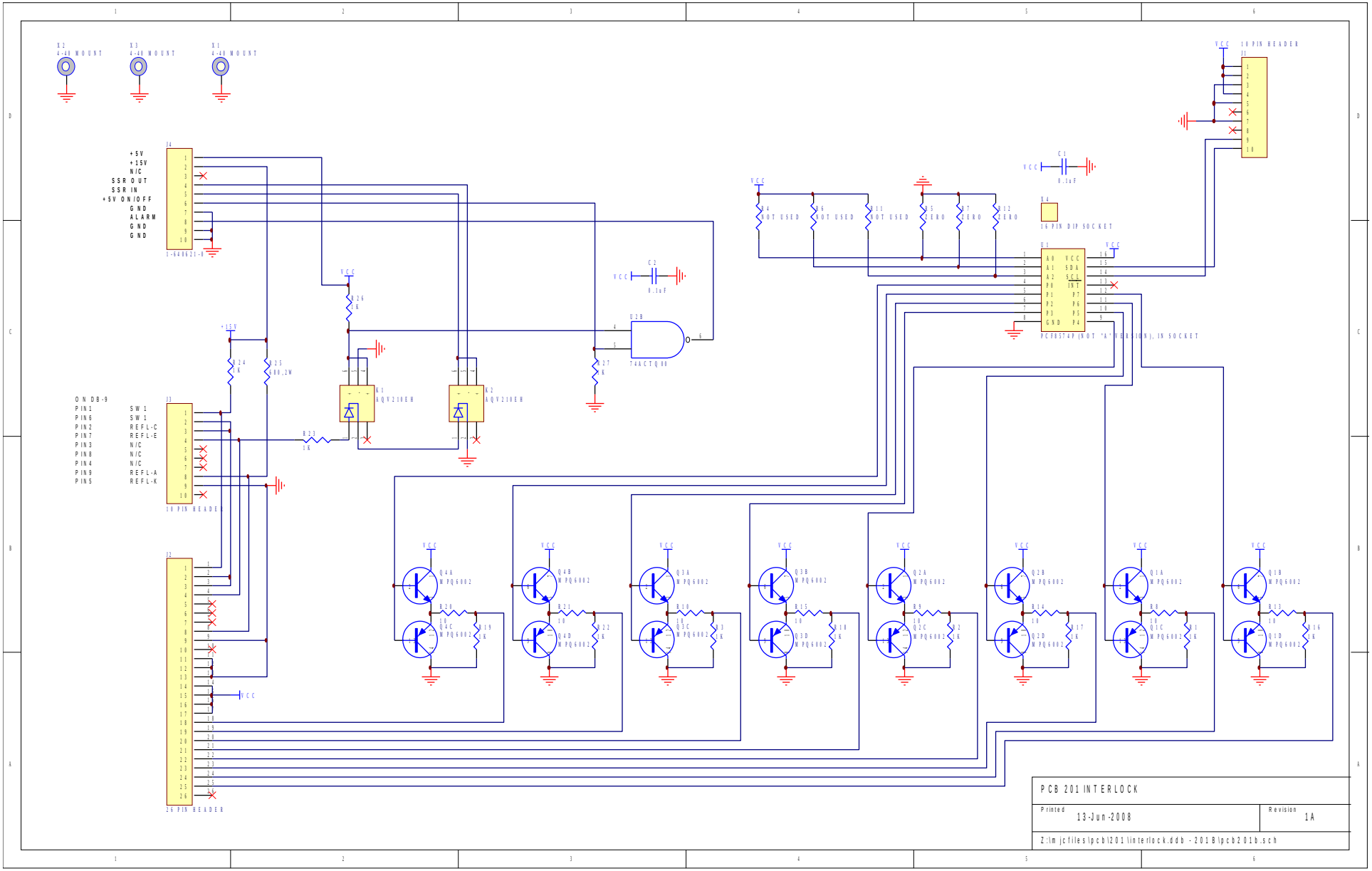


PCB 104E - KEYPAD / DISPLAY BOARD, 3/3

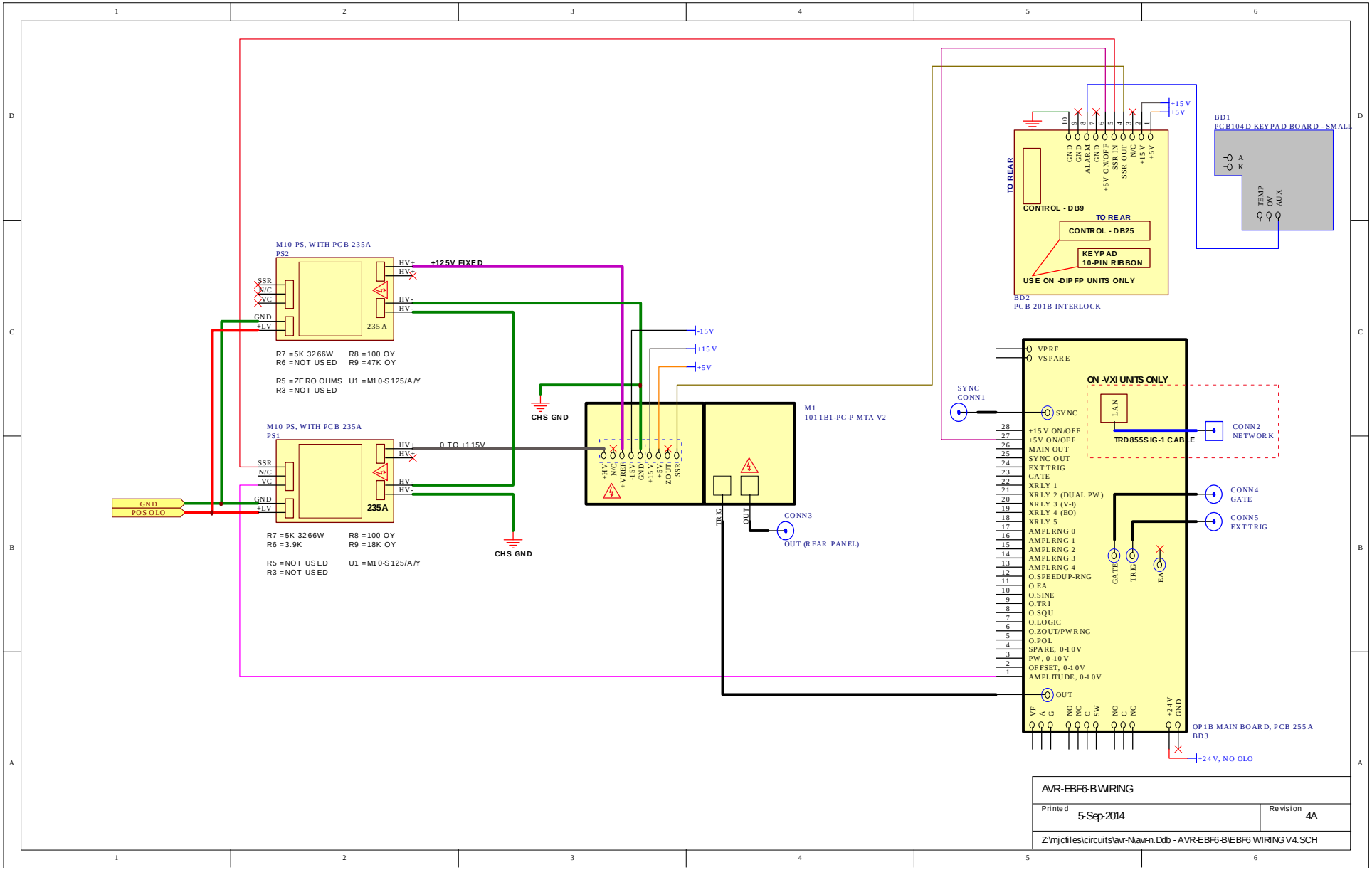


Title	LCD CIRCUITS, MECHANICAL
Date	3-Mar-2011
Revision	
Z:\mjcfiles\pcb\104e\keypad-2010.ddb - Documents\LCD-BUTT.SCH	

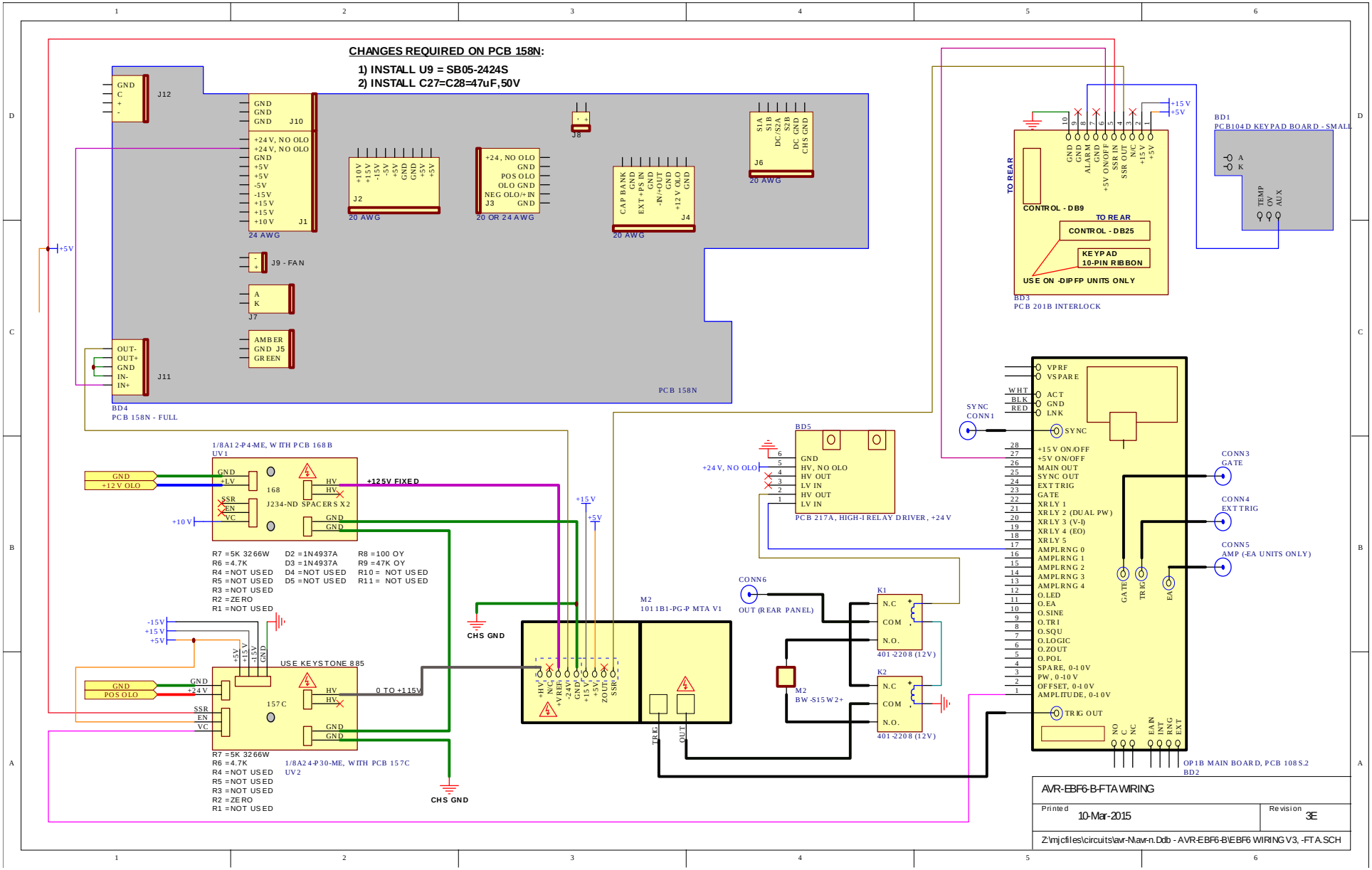
PCB 201B - INTERLOCK CONTROL



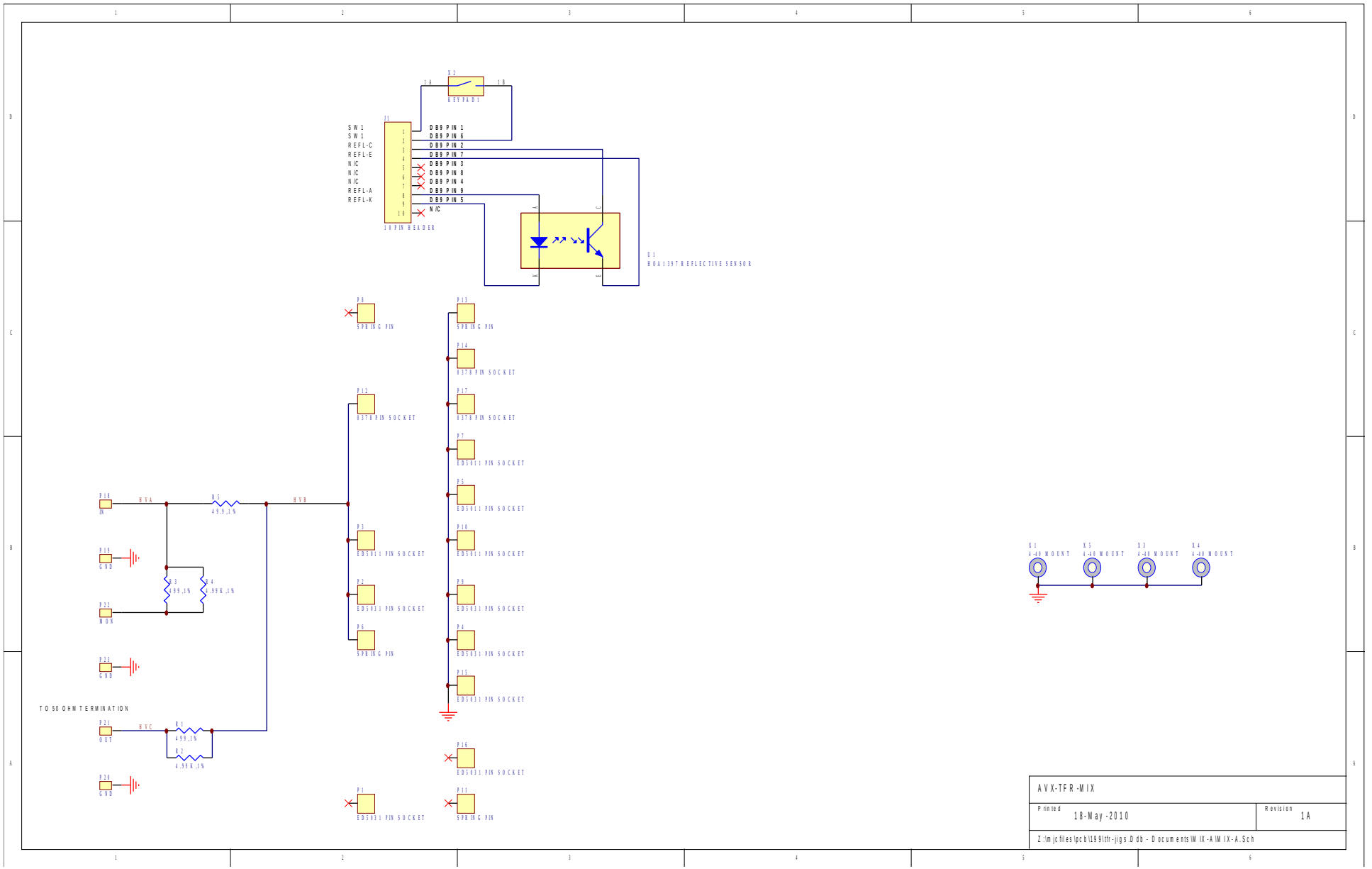
MAIN WIRING, STANDARD MODELS



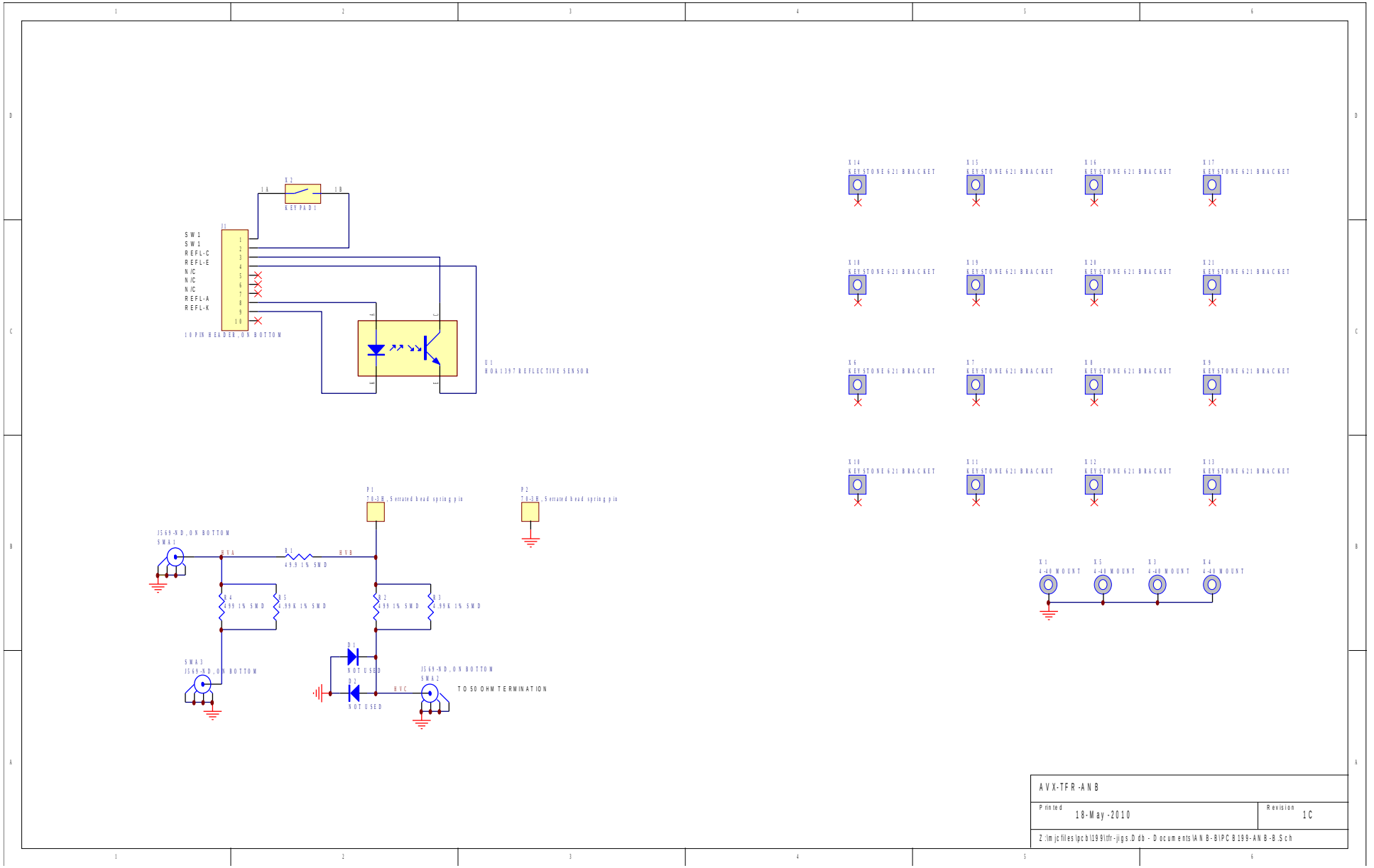
MAIN WIRING, -FTA MODELS



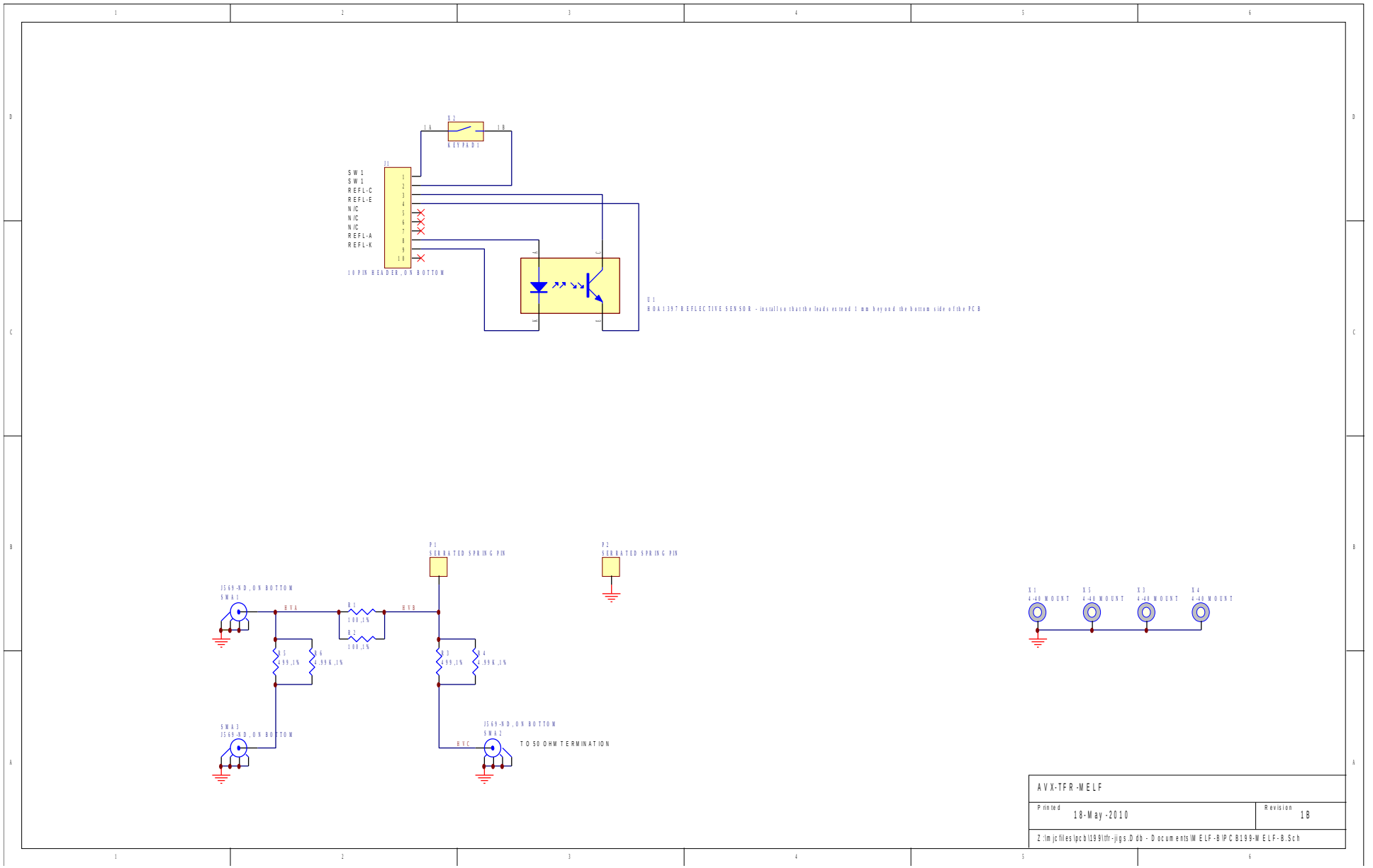
TEST JIG WIRING (AVX-TFR-MIX)



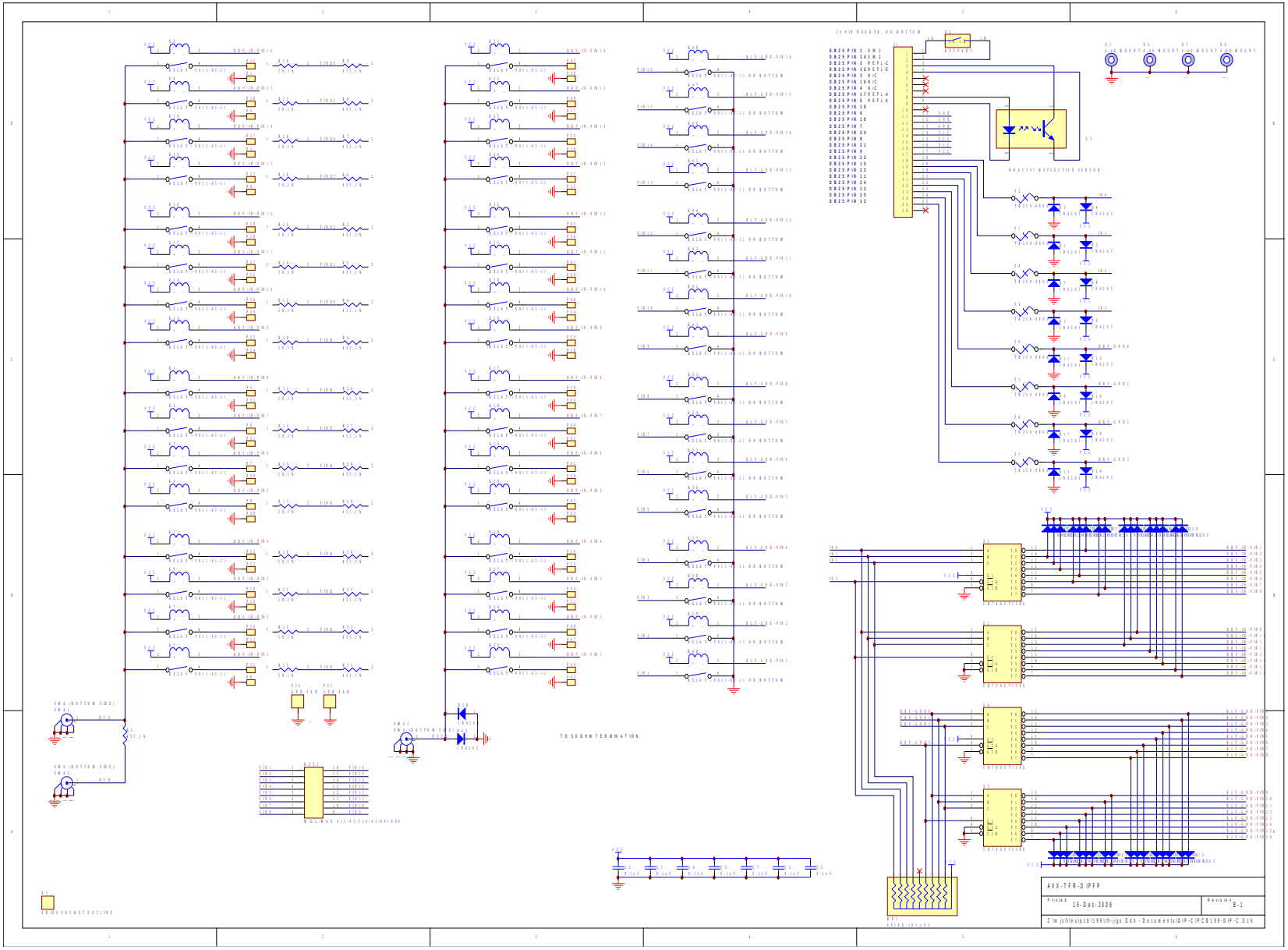
TEST JIG WIRING (AVX-TFR-ANB)



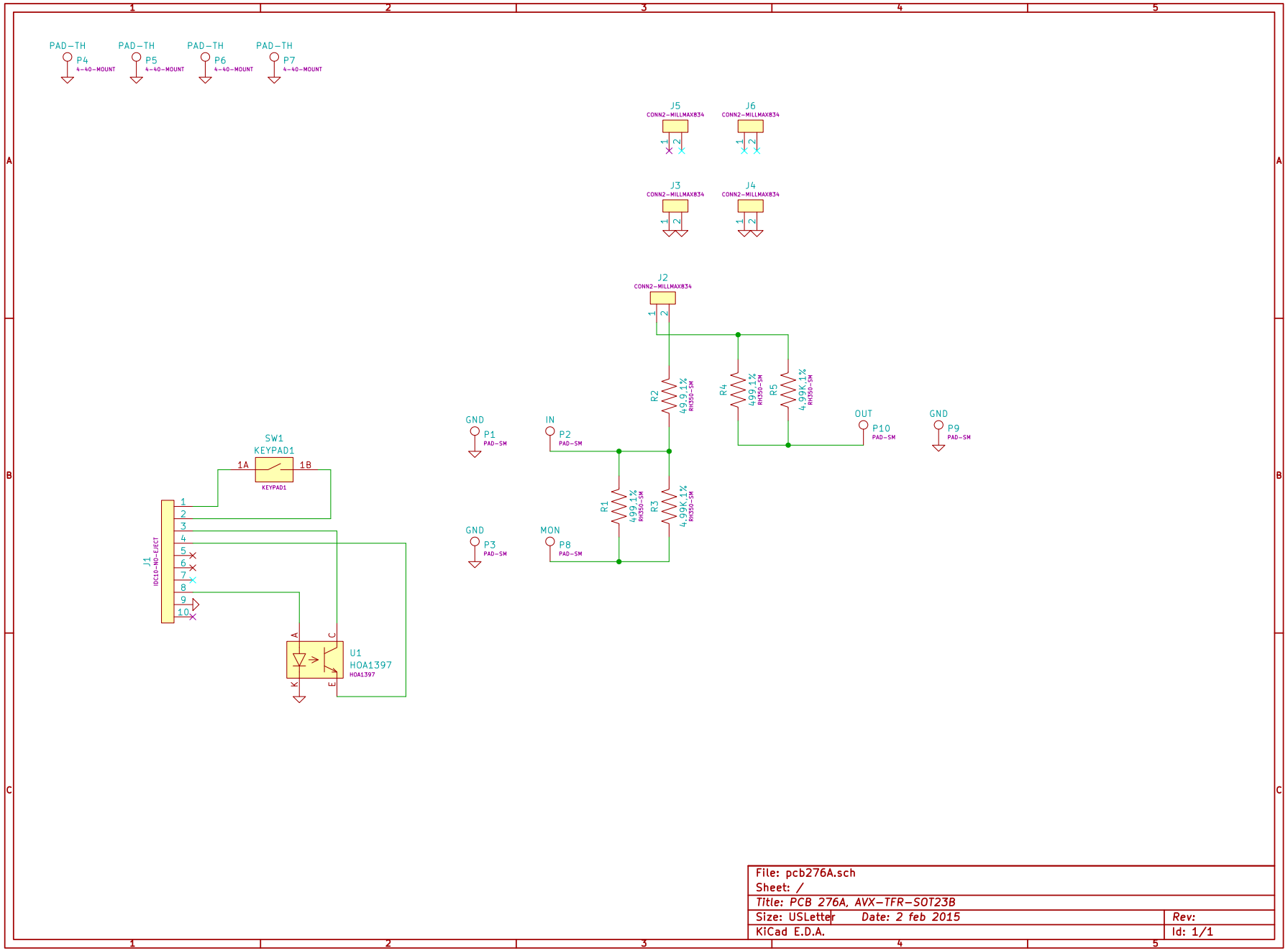
TEST JIG WIRING (AVX-TFR-MELF)



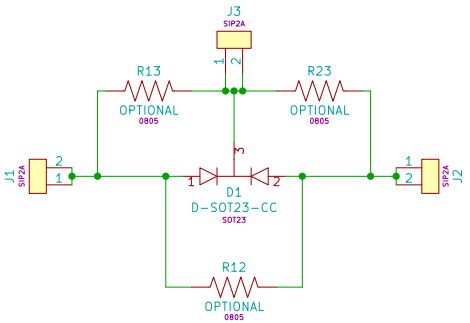
TEST JIG WIRING (AVX-TFR-DIPFP)



TEST JIG WIRING (AVX-TFR-SOT23B)



CUSTOMIZED DAUGHTERBOARD FOR AVX-TFR-SOT23B



AVTECH ELECTROSYSTEMS LTD.	
File: pcb274a.sch	
Sheet: /	
Title: DAUGHTERBOARD FOR AVX-CA-SOT23B	
Size: USLetter Date: 19 feb 2015	Rev:
KiCad E.D.A.	Id: 1/1

PERFORMANCE CHECK SHEET