INSTRUCTIONS

MODEL AVX-FD3-PS-IP-BNLA

0 to 250 MHz
FREQUENCY DIVIDER

WITH DIVISION FACTOR
VARIABLE FROM 2 TO 65535
AND A RESET INPUT

SERIAL NUMBER: _____

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

TECHNICAL SUPPORT

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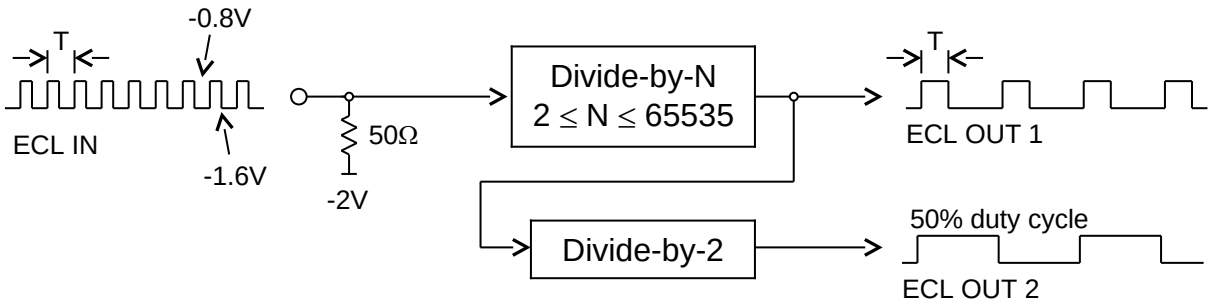
Manual Reference: /fileserver1/officefiles/instructword/avx-fd/OBS/AVX-FD3-PS-IP-BNLA.doc, created June 24, 1999

INTRODUCTION

The AVX-FD3-PS-IP-BNLA is a high-speed frequency divider that can operate at pulse repetition frequencies up to 250 MHz. The main output can be set to generate a pulse for every N input pulses, where N can vary from 2 to 65535. The output pulse width is equal, approximately, to one input period. A second output is also available, which generates a pulse for every 2N input pulses. This output has 50% duty cycle.

All outputs are ECL-level (i.e. logic high = -0.8V, logic low = -1.6V). The outputs can drive loads of 50Ω to ground or 50Ω to -2V, for maximum flexibility. The input can be set to accept ECL levels, or a 0.1V to 5.0V peak-to-peak pulse or sinewave signal.



Block Diagram of AVX-FD3-PS-IP-BNLA

SPECIFICATIONS

Model:	AVX-FD3-PS-IP-BNLA
Input Pulse Repetition Frequency (PRF):	0 - 250 MHz
Division Factor:	2 to 65535
Input Levels:	ECL (-0.8V and -1.6V), or a pulse or sinewave signal with 0.1 to 5 V peak-to-peak amplitude
Input Termination:	50Ω to -2V for ECL inputs, 50Ω to GND for 0.1 to 5 V peak-to-peak mode.
Input Pulse Width:	> 1 ns
Pulse width:	5 to 100 ns
Output Levels:	ECL (-0.8V and -1.6V)
Outputs:	OUT 1: $f_{OUT1} = f_{IN}/N$ OUT 2: $f_{OUT2} = f_{OUT1}/2$
Output Pulse Width:	OUT1: one input period, i.e. $PW_{OUT1} = 1/f_{IN}$ OUT2: 50% duty cycle, i.e. $PW_{OUT2} = 1/f_{OUT1}$
Jitter: (Ext trig in to pulse out)	≤ 100 ps
Connectors:	BNC
Power requirements:	120/240 Volts (switchable) 50-60 Hz
Dimensions:	100 mm x 215 mm x 375 mm (3.9” x 8.5” x 14.8”)
Temperature range:	+ 10° to + 40° C

INSTALLATION

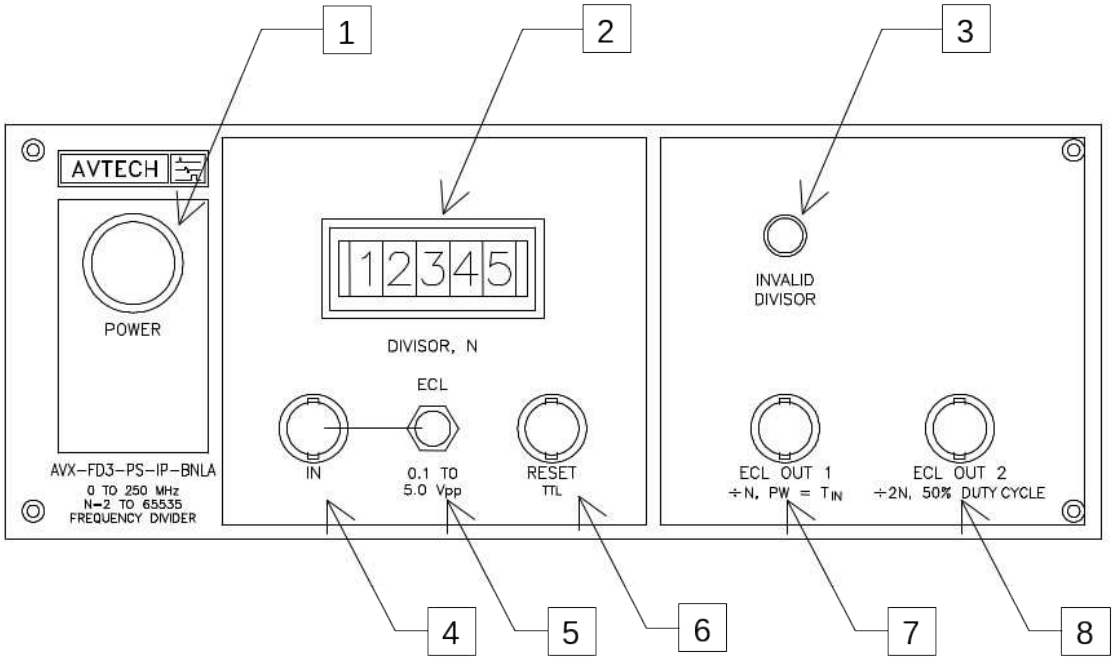
VISUAL CHECK

After unpacking the instrument, examine to ensure that it has not been damaged in shipment. Visually inspect all connectors, knobs, and the handles. Confirm that a power cord and this manual are with the instrument. If the instrument has been damaged, file a claim immediately with the company that transported the instrument.

PLUGGING IN THE INSTRUMENT

Examine the rear of the instrument. There will be a male power receptacle, a fuse holder and the edge of the power selector card visible. Confirm that the power selector is in the correct orientation - it should be marked either 120 or 240, indicating whether it expects 120V AC or 240V AC. If it is not set for the proper voltage, remove the fuse and then grasp the card with a pair of pliers and remove it. Rotate horizontally through 180 degrees. Reinstall the card and the correct fuse. In the 120V setting, a 1/2A slow blow fuse is required. In the 240V setting, a 1/4A slow blow fuse is required.

FRONT PANEL CONTROLS



1. POWER Switch. The POWER push button switch applies AC prime power to the primaries of the transformer, turning the instrument on. The push button lamp (#382 type) is connected to the internal +15V DC supply.

2. DIVISOR Thumbwheel Switch. This switch sets the division factor, N. For normal operation, this value can be set between 2 and 65535. For values above 65535, no output will be generated, and the "Invalid Divisor" light (item 3) will turn on.

3. INVALID DIVISOR Light. This indicator comes on when the divisor is set to a value greater than 65535.

4. IN Connector. The input signal is applied to this BNC connector.

5. ECL / 0.1 to 5.0 Vpp Switch. This switch determines the operating mode of the IN connector.

   When this switch is in the "ECL" position, the IN connector is terminated with a 50Ω shunt resistance to -2V (which is a standard termination for ECL logic circuits). ECL logic levels (i.e. -0.8V and -1.6V) are required to trigger the instrument.

   When this switch is in the "0.1 to 5.0 Vpp" position, the IN connector is terminated with a 50Ω shunt resistance to ground. A pulse or sinewave signal with amplitude

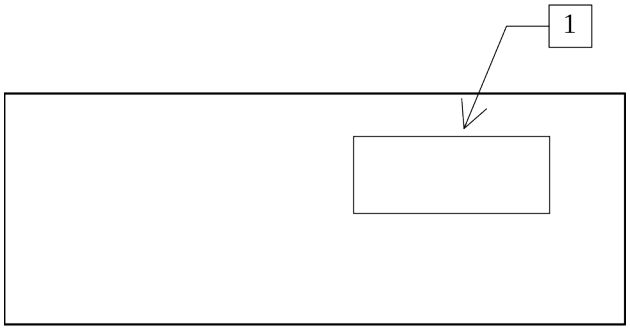
between 0.1 and 5.0 Volts peak-to-peak is required to trigger the instrument.

6. RESET CONNECTOR. A TTL-level pulse on this input will reset the internal counters to a default state. This can be used for synchronisation purposes.

7. ECL OUT 1. This connector supplies the main output. The pulse repetition frequency of this output is 1/N of the input pulse repetition frequency. The output levels are ECL (i.e. -0.8V and -1.6V). This output should be terminated by a 50Ω load to ground or -2V. The pulse width of this output is equal to one period of the input signal.

8. ECL OUT 2. This connector supplies the secondary output. The pulse repetition frequency of this output is 1/2 of the "ECL OUT 1" output pulse repetition frequency. The duty cycle of this output is 50%.

REAR PANEL CONTROLS

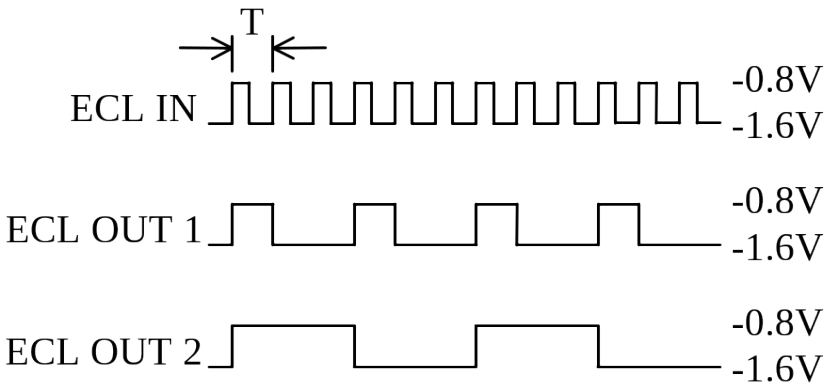


1. AC POWER INPUT. A three-pronged recessed male connector is provided on the back panel for AC power connection to the instrument. Also contained in this assembly is a 0.5A slow blow fuse and a removable card that can be removed and repositioned to switch between 120V AC in and 240V AC in.

GENERAL INFORMATION

OPERATION FOR 2 ≤ N ≤ 65535

The figure below shows the basic relationship between the input signal and the two outputs, for 2 ≤ N ≤ 65535. The main output, ECL OUT 1, generates a pulse for every N input cycles, and the output pulse width is approximately equal to one input period ("T"). The second output, ECL OUT 2, generates a pulse for every 2N input cycles. It has 50% duty cycle.



Inputs and Outputs For N=3

OPERATION FOR N > 65535

If N is set greater than 65535, no output will be generated (i.e. the outputs will remain at ECL logic low, -1.6V), and the "Invalid Divisor" indicator will light.

OPERATION FOR N = 0

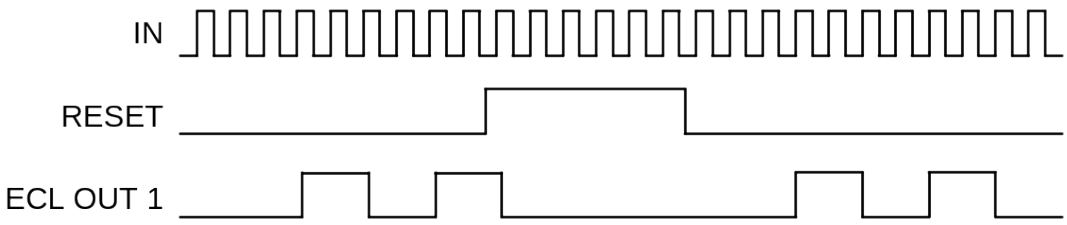
If N is set to zero, no output will be generated (i.e. the outputs will remain at ECL logic low, -1.6V). The "Invalid Divisor" indicator will not light.

OPERATION FOR N = 1

The divider operates slightly differently for N = 1. In this case, the internal divider circuitry is bypassed, and the input is routed directly to the ECL OUT 1 output (after passing through a buffer stage). The output pulse width is approximately equal to the input pulse width. Note that if the input pulse width is very narrow, the buffer circuit may not be able to respond quickly enough. (This mode is an extra feature that is not included in the specifications.)

-BNLA OPTION

The "-BNLA" option adds a reset input to the front panel, which can be used for synchronization, as shown below:



In this example, N=4. When the reset input is TTL high, the internal counter are reset to zero and are held at zero until the reset input switches to TTL low. An output pulse is generated on the fourth input pulse after the reset line returns to TTL low.

OUTPUT TERMINATION

Both outputs should be terminated with a 50Ω load, for minimum waveform distortion. The load can be connected to ground or -2V, as desired. (The former is a typical termination for pulse generators, and the latter is a common ECL-specific termination.)

TOP COVER REMOVAL

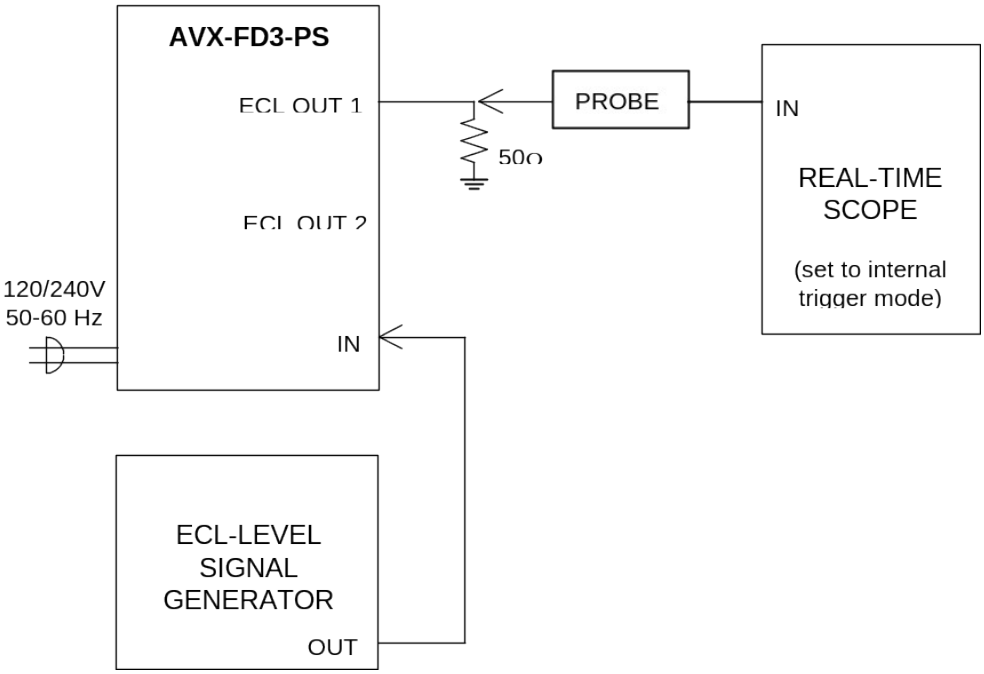
The interior of the instrument may be accessed by removing the four Phillips screws on the top panel. With the four screws removed, the top cover may be slid back (and off).

ELECTROMAGNETIC INTERFERENCE

To prevent electromagnetic interference with other equipment, all used outputs should be connected to shielded 50Ω loads using shielded 50Ω coaxial cables. Unused outputs should be terminated with shielded 50Ω BNC terminators or with shielded BNC dust caps, to prevent unintentional electromagnetic radiation. All cords and cables should be less than 3m in length.

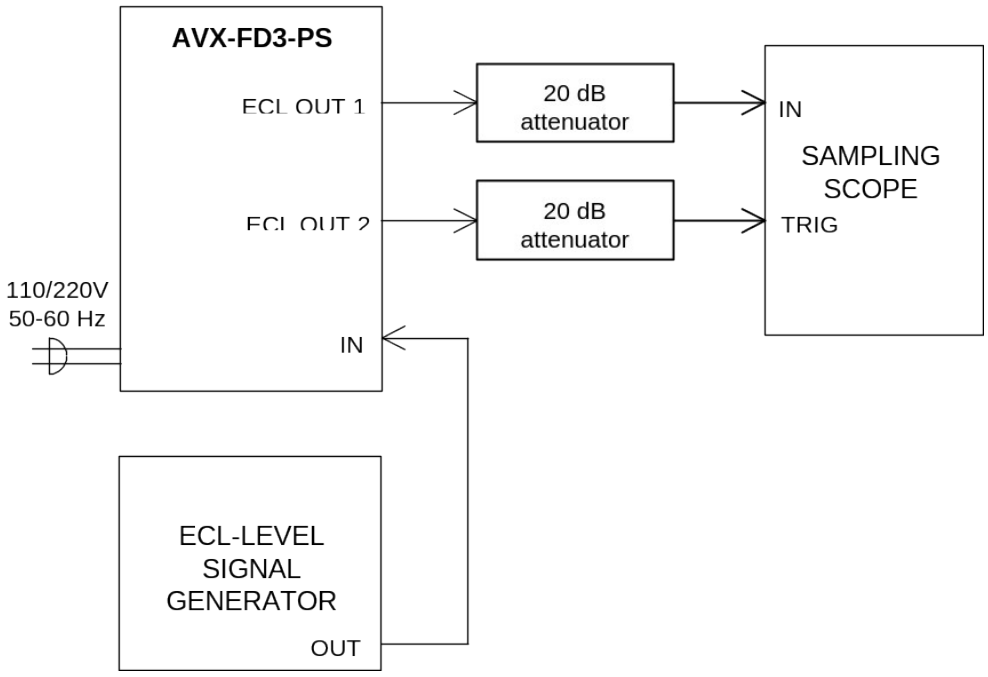
GENERAL TEST ARRANGEMENT

The diagram below illustrates the basic technique for testing the AVX-FD3-PS-IP-BNLA with a real-time oscilloscope. Use an oscilloscope with sufficient bandwidth to observe your signal.



Test Arrangement for Real-Time Scopes

If you wish to test the divider at its maximum rated pulse repetition frequency (250 MHz), you may need to use a sampling oscilloscope, in which case the arrangement in the following figure suggested. In this arrangement, the main output is terminated by the 50Ω input impedance of the sampling scope, and the scope is triggered by the secondary output.



Test Arrangement for Sampling Scopes

PERFORMANCE CHECKSHEET