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SINCE 1975

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## INSTRUCTIONS

MODEL AVD-1000-C-ESA MONOCYCLE GENERATOR

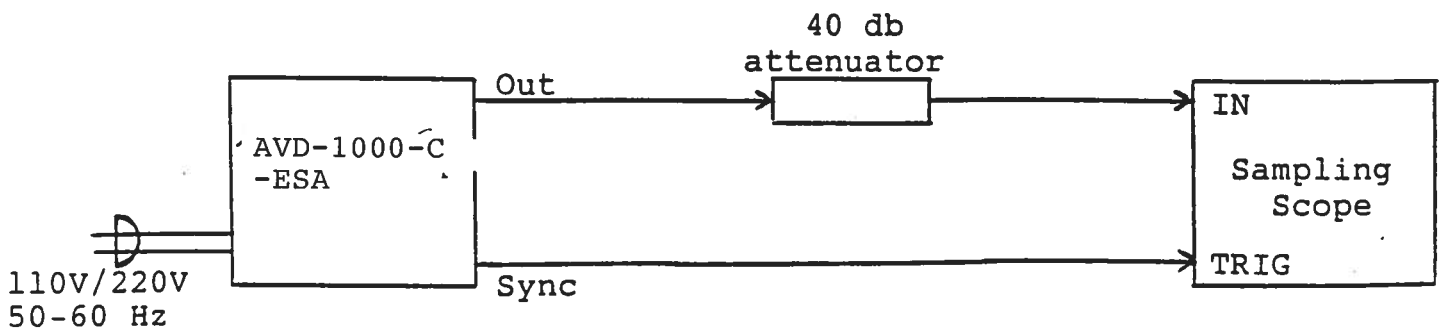
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## WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been disassembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

Fig. 1

MONOCYCLE GENERATOR TEST ARRANGEMENT



Notes:

- 1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed ten gigahertz.
- 2) The use of 40 db attenuator at the sampling scope vertical input channel will insure a peak input signal to the sampling scope of less than one volt.
- 3) The sync output channel provides a 500 mV 20 nsec wide pulse to fifty ohms. The sampling scope should be set to trigger on the positive edge of the sync pulse.
- 4) To obtain a stable output display the front panel TRIG toggle switch should be in the INT position. The DELAY control and the scope triggering controls are then adjusted to obtain a stable output.
- 5) The output PRF may be varied from about 2 MHz to 5 MHz using the rear panel one turn control. The unit was shipped with the PRF set at 5.0 MHz.
- 6) An external clock may be used to control the output PRF of the AVD unit by setting the front panel TRIG toggle switch in the EXT position and applying a 0.2 usec (approx.) TTL level pulse to the TRIG BNC connector input. For operation in this mode, the scope time base must also be triggered by the external clock rather than from the SYNC output.

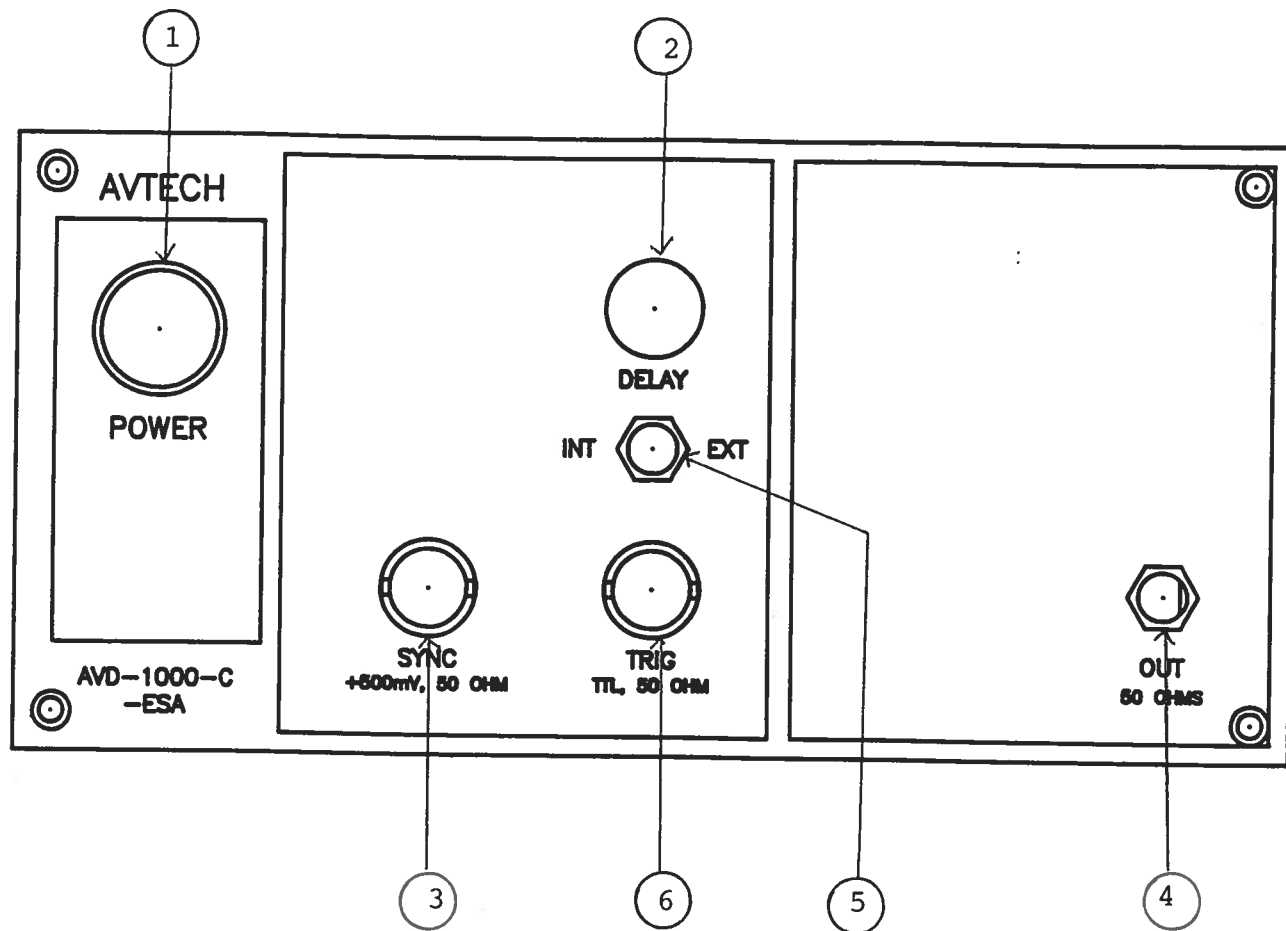


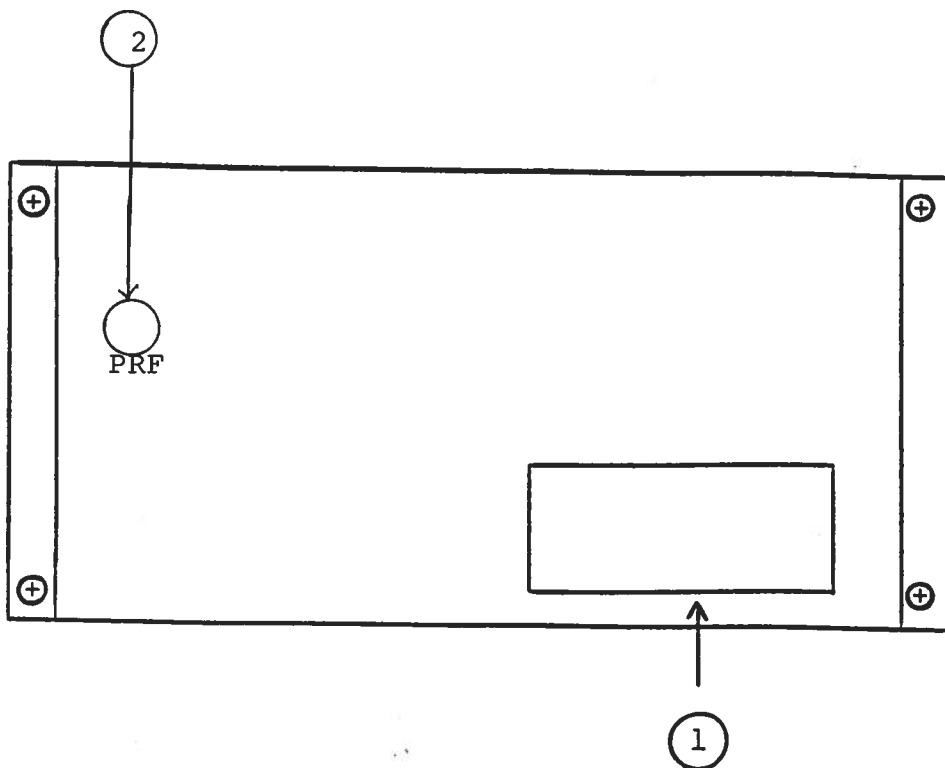
Fig. 2

FRONT PANEL CONTROLS

- (1) ON-OFF Switch. Applies basic prime power to all stages.
- (2) DELAY Control. Controls the relative delay between the reference output pulse provided at the SYNC output (4) and the main output (6). This delay is variable over the range of 0 to about 150 ns.
- (3) SYNC Output. This output precedes the main output (6) and is used to trigger the scope time base. The output is a 500 mV 20 ns (approx.) pulse capable of driving a fifty ohm load. Set scope to trigger on positive edge.
- (4) OUT Connector. SMA connector provides output to a fifty ohm load.
- (5) EXT-INT Control. With this toggle switch in the INT position, the PRF of the AVH unit is controlled via an internal clock (fixed at 5.0 MHz). With the toggle switch in the EXT position, the AVD unit requires a 0.1 us TTL level pulse applied at the TRIG input in order to trigger the output stages. In addition, in this mode, the scope time base must be triggered by the external trigger source.
- (6) TRIG Input. The external trigger signal is applied at this input when the EXT-INT toggle switch is in the EXT position.

Fig. 3

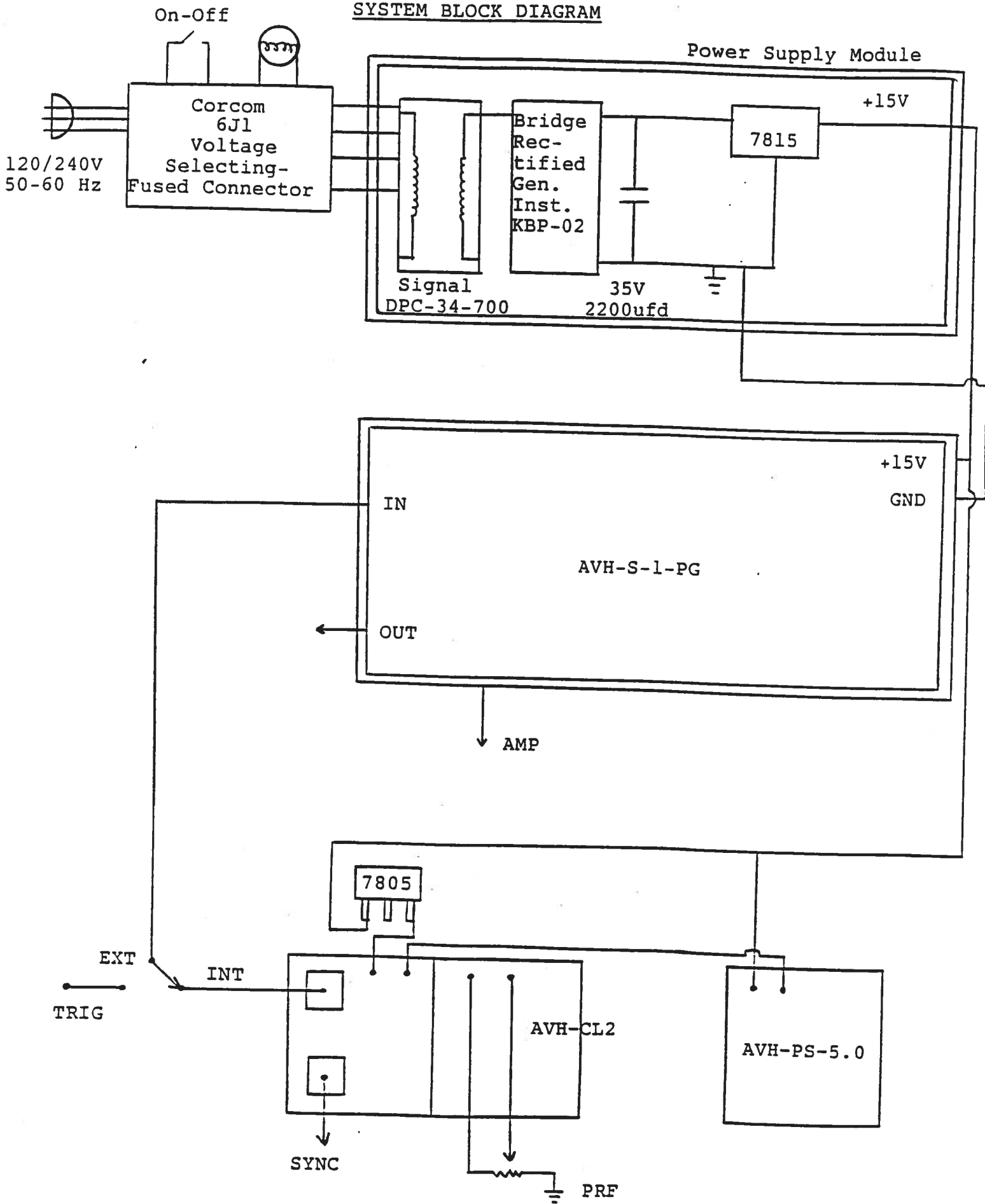
BACK PANEL CONTROLS



- (1) FUSED CONNECTOR, VOLTAGE SELECTOR. The detachable power cord is connected at this point. In addition, the removable cord is adjusted to select the desired input operating voltage. The unit also contains the main power fuse (0.25 A SB).
- (2) PRF CONTROL. One turn locking control allows the internal clock PRF to be varied from about 2.0 MHz to 5.0 MHz.



SYSTEM BLOCK DIAGRAM



## SYSTEM DESCRIPTION AND REPAIR PROCEDURE

The AVD-C consists of a pulse generator module (AVD-C) a clock module (AVD-CL2) and a power supply board which supplies +15 volts (600 mA max) to the pulse generator module. In the event that the unit malfunctions, remove the instrument cover by removing the four Phillips screws on the back of the unit. The top cover may then be slid off. Measure the voltage at the +15V pin of the PG module. If this voltage is substantially less than +15 volts, unsolder the line connecting the power supply and PG modules and connect 50 ohm 10 W load to the PS output. The voltage across this load should be about +15 V DC. If this voltage is substantially less than 15 volts the PS module is defective and should be repaired or replaced. If the voltage across the resistor is near 15 volts, then the PG module should be replaced or repaired. The sealed PG module must be returned to Avtech for repair (or replacement). The clock module provides a 0.1 usec TTL level trigger pulse at pin 2 to trigger the PG module and a 0.1 usec TTL level synch pulse at pin 3 to trigger the sampling scope display device. The output at pin 3 precedes the output at pin 2 by almost 0 to 100 nsec depending on the DELAY control setting. The clock module is powered by +15V. With the INT-EXT switch in the EXT position, the clock module is disconnected from the PG module. The clock module is functioning properly if:

- a) 0.1 us TTL level outputs are observed at pins 2 and 3.
- b) The PRF of the outputs can be varied over the range of 5 MHz using the PRF control.
- c) The relative delay between the pin 2 and 3 outputs can be varied by at least 100 ns by the DELAY control.

The sealed clock module must be returned to Avtech for repair or replacement if the above conditions are not observed.

March 22/94

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