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INSTRUCTIONS

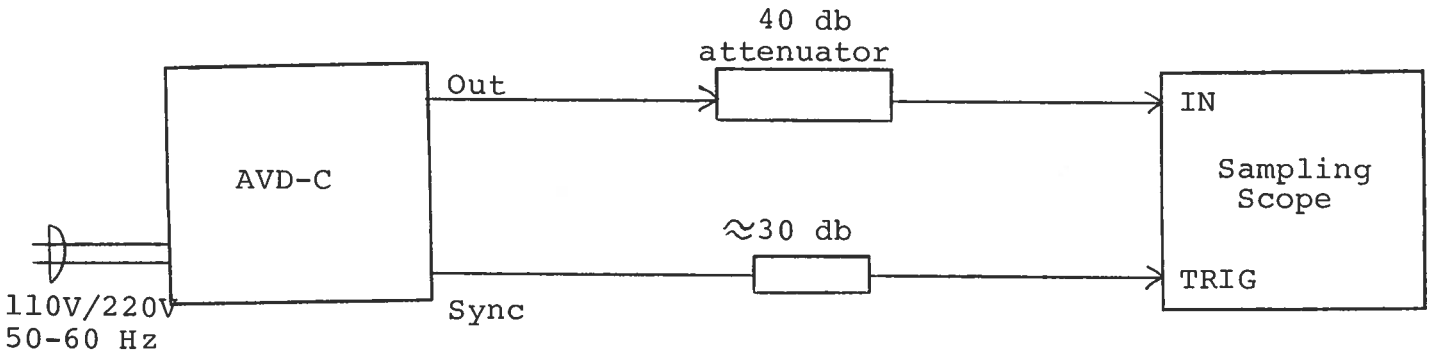
MODEL AVD-C-OS PULSE GENERATOR

S.N.:

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

Fig. 1 PULSE GENERATOR TEST ARRANGEMENT



Notes:

1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed one gigahertz.

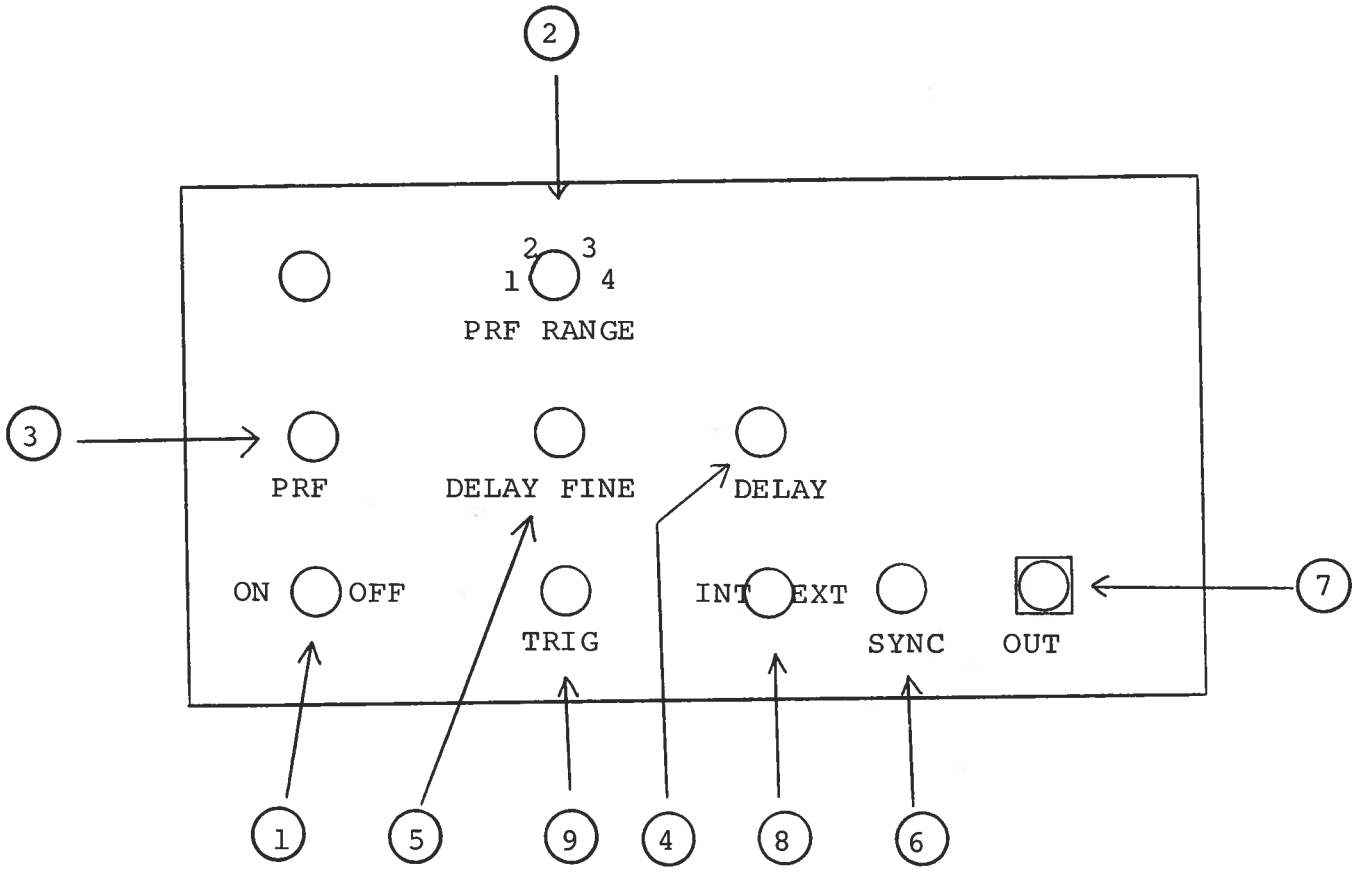
2) The use of 40 db attenuator at the sampling scope vertical input channel will insure a peak input signal to the sampling scope of less than one volt.

3) The sync output channel provides TTL level signals. To avoid overdriving the TRIG input channel of some sampling scopes, a 30 db attenuator should be placed at the input to the sampling scope trigger channel.

4) To obtain a stable output display the PRF control on the front panel should be set mid-range while the PRF range switch may be in either range. The front panel TRIG toggle switch should be in the INT position. The front panel DELAY controls and the scope triggering controls are then adjusted to obtain a stable output. The scope may then be used to set the desired PRF by rotating the PRF control and by means of the PRF range switch.

5) DC OFFSET Input. To DC offset the output pulse, connect a DC power supply set to the desired offset value to these terminals. The maximum allowable DC offset voltage is ±50 volts. (option).

Fig. 2 FRONT PANEL CONTROLS



(1) ON-OFF Switch. Applies basic prime power to all stages.

(2) PRF Control. The PRF RANGE and PRF controls determine
(3) output PRF as follows:

	PRF MIN	PRF MAX
Range 1	100 Hz	1 KHz
Range 2	1 KHz	10 KHz
Range 3	10 KHz	100 KHz
Range 4	100 KHz	1 MHz

(4) DELAY Controls. Controls the relative delay between the
(5) reference output pulse provided at the SYNC output (6) and the main output (7). This delay is variable over the range of 0 to at least 500 nsec.

(6) SYNC Output. This output precedes the main output (7) and is used to trigger the sampling scope time base. The output is a TTL level 100 nsec (approx) pulse capable of driving a fifty ohm load.

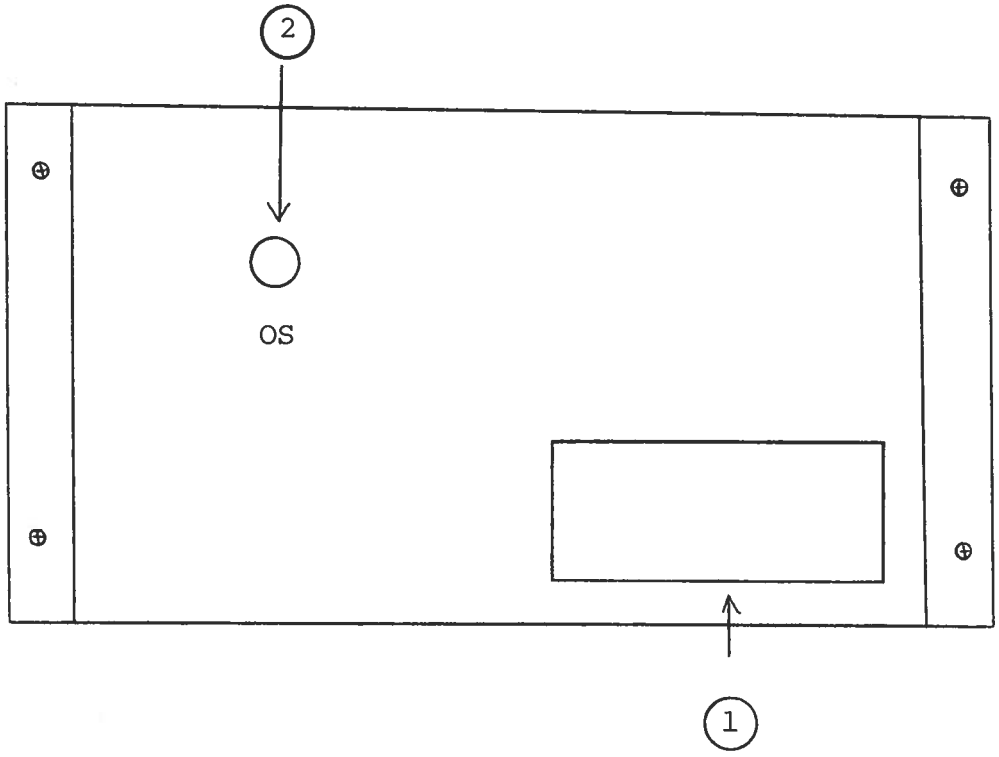
(7) OUT. SMA output connect provides output to a fifty ohm load.

(8) EXT-INT Control. With this toggle switch in the INT position, the PRF of the AVD unit is controlled via an internal clock which in turn is controlled by the PRF controls. With the toggle switch in the EXT position, the AVD unit requires a 0.2 usec TTL level pulse applied at the TRIG input in order to trigger the output stages. In addition, in this mode, the scope time base must be triggered by the external trigger source.

(9) TRIG Input. The external trigger signal is applied at this input when the EXT-INT toggle switch is in the EXT position.

Fig. 3

BACK PANEL CONTROLS

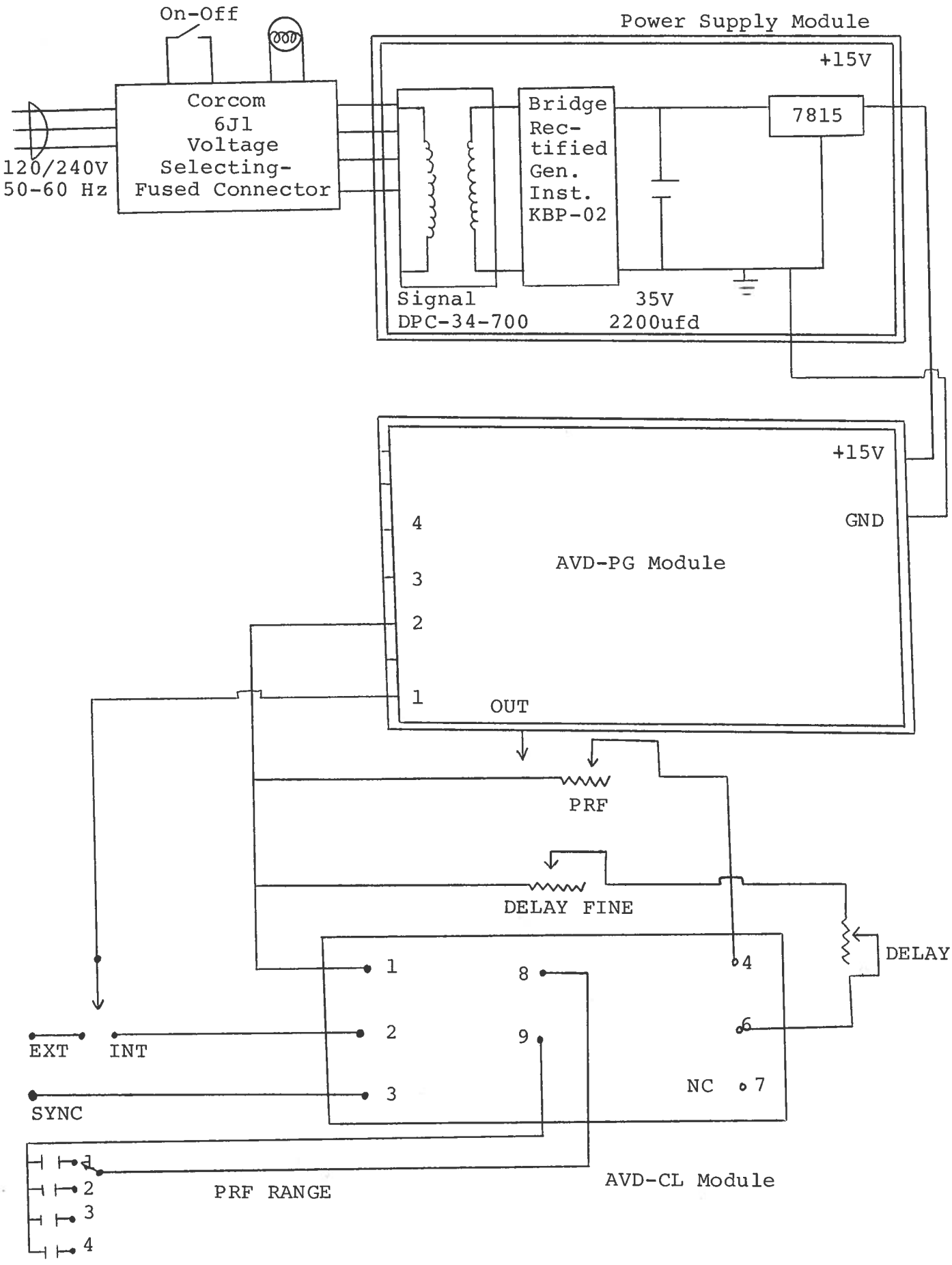


(1) FUSED CONNECTOR, VOLTAGE SELECTOR. The detachable power cord is connected at this point. In addition, the removable cord is adjusted to select the desired input operating voltage. The unit also contains the main power fuse.

(2) DC OFFSET Input. To DC offset the output pulse, connect a DC power supply set to the desired offset value to these terminals. The maximum allowable DC offset voltage is ±50 volts. (option).

Fig. 4

SYSTEM BLOCK DIAGRAM



SYSTEM DESCRIPTION AND REPAIR PROCEDURE

The AVD-C consists of a pulse generator module (AVD-PG), a clock module (AVD-CL) and a power supply board which supplies +15 volts (600 mA max) to the pulse generator module. In the event that the unit malfunctions, remove the instrument cover by removing the four Phillips screws on the back of the unit. The top lid may then be slid off. Measure the voltage at the +15V pin of the PG module. If this voltage is substantially less than +15 volts, unsolder the line connecting the power supply and PG modules and connect 50 ohm 10 W load to the PS output. The voltage across this load should be about +15V DC. If this voltage is substantially less than 15 volts the PS module is defective and should be repaired or replaced. If the voltage across the resistor is near 15 volts, then the PG module should be replaced or repaired. The sealed PG module must be returned to Avtech for repair (or replacement). The clock module provides a 0.1 usec TTL level trigger pulse at Pin 2 to trigger the PG module and a 0.1 usec TTL level sync pulse at Pin 3 to trigger the sampling scope display device. The output at Pin 3 precedes the output at Pin 2 by almost 0 to 100 nsec depending on the DELAY control setting. The clock module is powered by +5.8 V supplied by the PG module (from Pin 2 to Pin 1). With the INT-EXT switch in the EXT position, the clock module is disconnected from the PG module. The clock module is functioning properly if:

a) 0.1 usec TTL level outputs are observed at Pins 2 and 3.
b) The PRF of the outputs can be varied over the range of 1 KHz to 1 MHz using the PRF and PRF RANGE controls.
c) The relative delay between the Pin 2 and 3 outputs can be varied by at least 500 nsec by the DELAY control.

The sealed clock module must be returned to Avtech for repair or replacement if the above conditions are not observed.

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