AVTECH ELECTROSYSTEMS LTD.

NANOSECOND WAVEFORM ELECTRONICS
ENGINEERING – MANUFACTURING

P.O. BOX 265
OGDENSBURG
NEW YORK
13669
(315) 472-5270

BOX 5120, STN. "F"
OTTAWA, ONTARIO
CANADA K2C 3H4
TEL: (613) 226-5772
FAX: (613) 226-2802
TELEX: 053-4591

INSTRUCTIONS

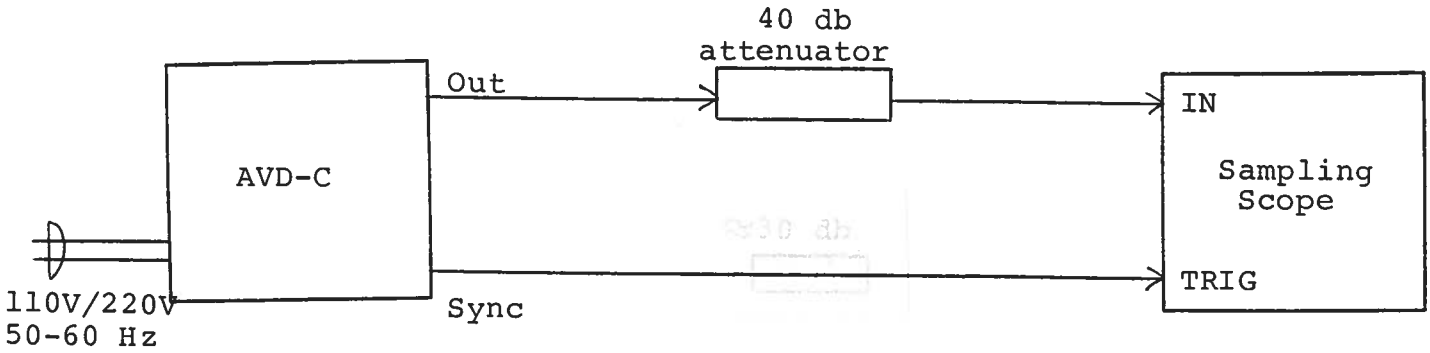
MODEL AVD-C-3000-NSW1 PULSE GENERATOR

S.N.:

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

Fig. 1 PULSE GENERATOR TEST ARRANGEMENT



Notes:

1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed 10 gigahertz.

2) The use of 40 db attenuator at the sampling scope vertical input channel will insure a peak input signal to the sampling scope of less than one volt.

3) The sync output channel provides a 500 mV 20 nsec wide pulse to fifty ohms. The sampling scope should be set to trigger on the positive edge of the sync pulse.

4) To obtain a stable output display the PRF control on the front panel should be set mid-range while the PRF range switch may be in either range. The front panel TRIG toggle switch should be in the INT position. The front panel DELAY controls and the scope triggering controls are then adjusted to obtain a stable output. The scope may then be used to set the desired PRF by rotating the PRF control and by means of the PRF range switch.

5) The unit may be tuned from about 2500 MHz to about 3300 MHz using the two ten turn TRIM pots shown below. Clockwise rotation of the right-hand pot tends to increase the period (or decrease the frequency) while clockwise rotation of the left-hand pot tends to decrease the period.

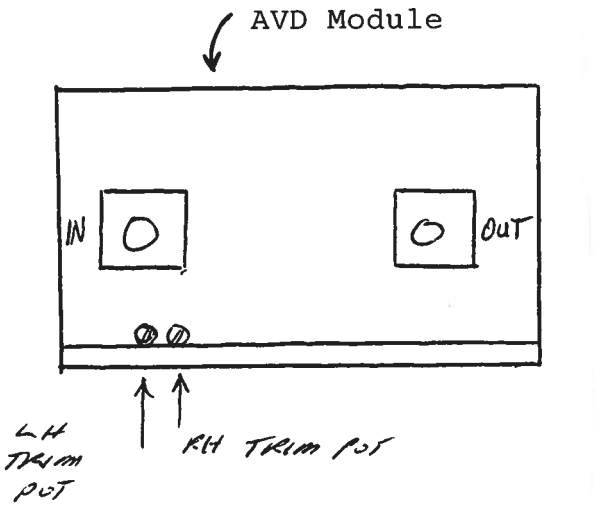
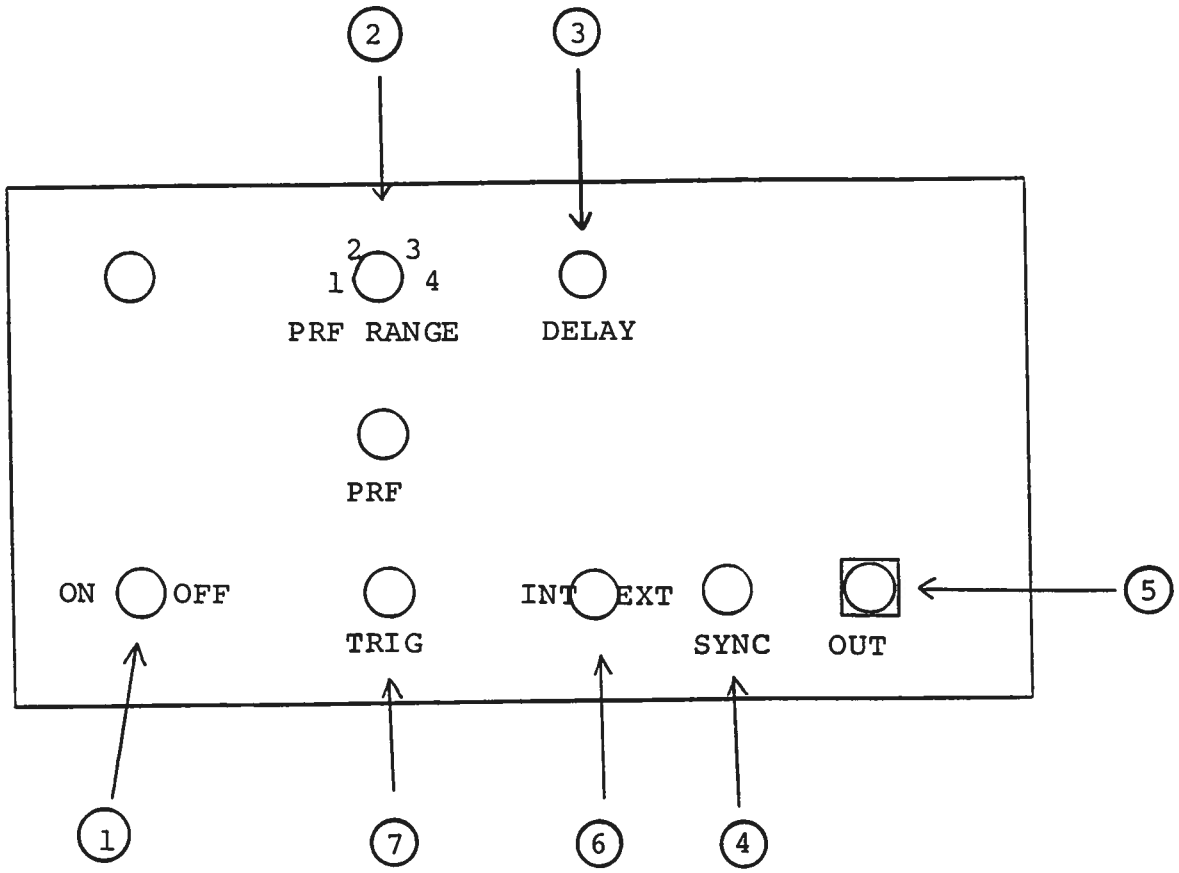


Fig. 2

FRONT PANEL CONTROLS



(1) ON-OFF Switch. Applies basic prime power to all stages.

(2) PRF Control. Varies PRF from 1.0 KHz to 1.0 MHz as follows:

Range 1	1.0 KHz		8 KHz
Range 2	8 KHz	to	40 KHz
Range 3	40 KHz	to	200 KHz
Range 4	200 KHz	to	1.0 MHz

(3) DELAY Control. Controls the relative delay between the reference output pulse provided at the SYNC output (4) and the main outputs (5) and (6). This delay is variable over the range of 0 to about 150 nsec.

(4) SYNC Output. This output precedes the main output (5) and is used to trigger the scope time base. The output is a 500 mV 20 nsec (approx.) pulse capable of driving a fifty ohm load. Set scope to trigger on positive edge.

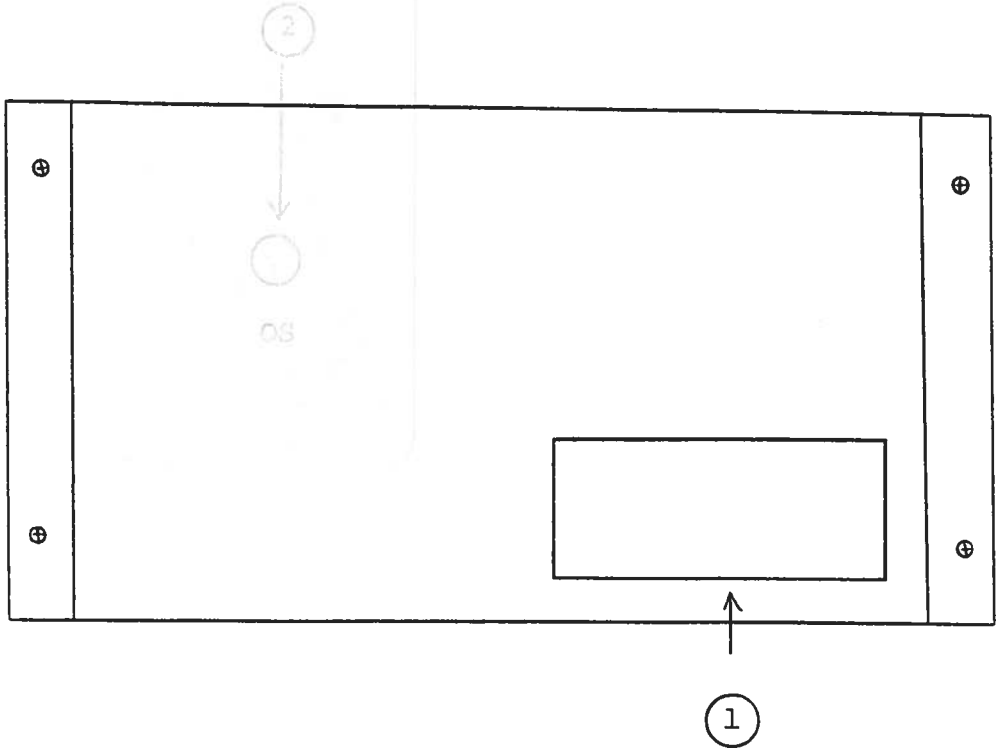
(5) OUT. SMA output connect provides output to a fifty ohm load.

(6) EXT-INT Control. With this toggle switch in the INT position, the PRF of the AVD unit is controlled via an internal clock which in turn is controlled by the PRF controls. With the toggle switch in the EXT position, the AVD unit requires a 0.2 usec TTL level pulse applied at the TRIG input in order to trigger the output stages. In addition, in this mode, the scope time base must be triggered by the external trigger source.

(7) TRIG Input. The external trigger signal is applied at this input when the EXT-INT toggle switch is in the EXT position.

Fig. 3

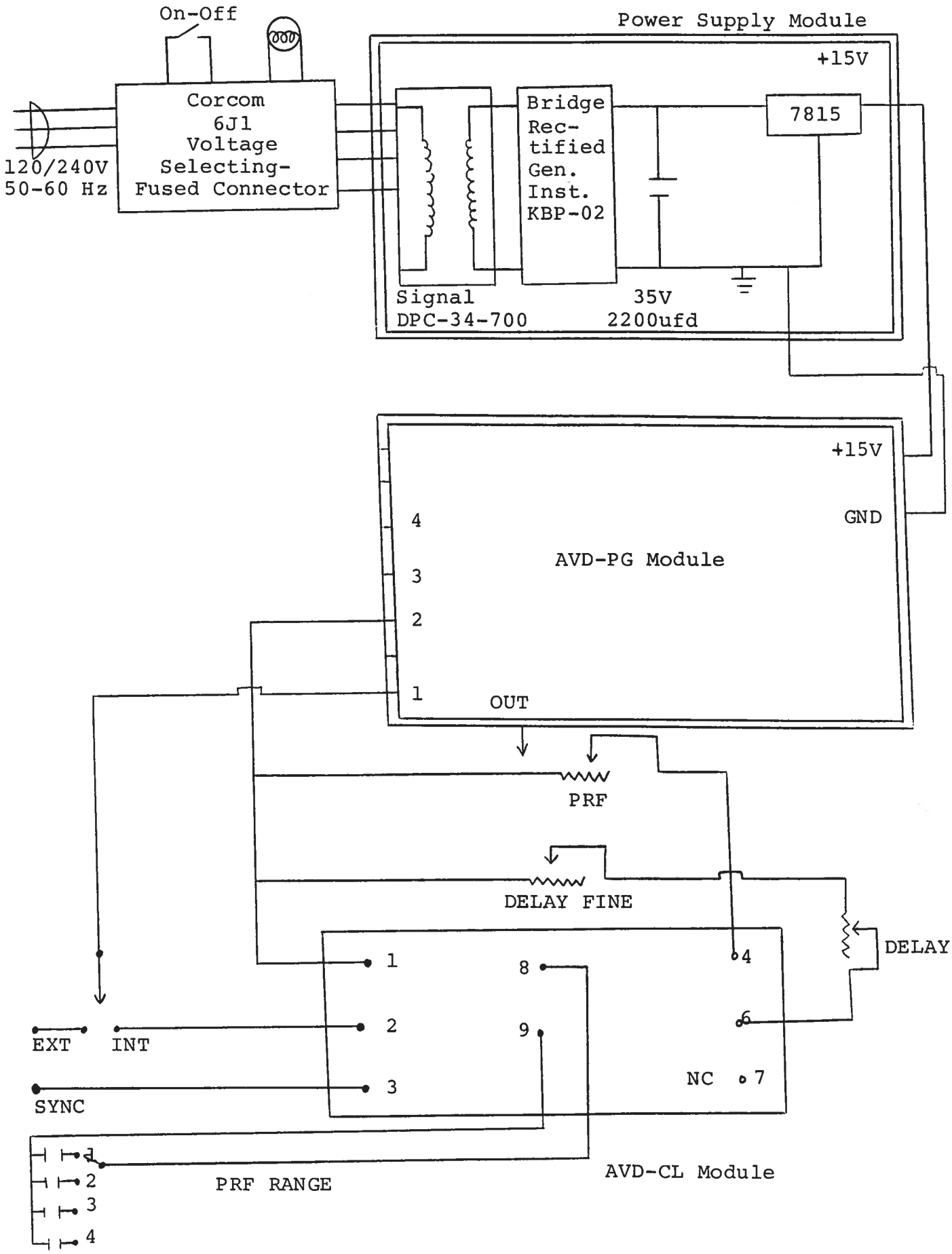
BACK PANEL CONTROLS



(1) FUSED CONNECTOR, VOLTAGE SELECTOR. The detachable power cord is connected at this point. In addition, the removable cord is adjusted to select the desired input operating voltage. The unit also contains the main power fuse.

Fig. 4

SYSTEM BLOCK DIAGRAM



SYSTEM DESCRIPTION AND REPAIR PROCEDURE

The AVD-C consists of a pulse generator module (AVD-PG), a clock module (AVD-CL) and a power supply board which supplies +15 volts (600 mA max) to the pulse generator module. In the event that the unit malfunctions, remove the instrument cover by removing the four Phillips screws on the back of the unit. The top lid may then be slid off. Measure the voltage at the +15V pin of the PG module. If this voltage is substantially less than +15 volts, unsolder the line connecting the power supply and PG modules and connect 50 ohm 10 W load to the PS output. The voltage across this load should be about +15V DC. If this voltage is substantially less than 15 volts the PS module is defective and should be repaired or replaced. If the voltage across the resistor is near 15 volts, then the PG module should be replaced or repaired. The sealed PG module must be returned to Avtech for repair (or replacement). The clock module provides a 0.1 usec TTL level trigger pulse at Pin 2 to trigger the PG module and a 0.1 usec TTL level sync pulse at Pin 3 to trigger the sampling scope display device. The output at Pin 3 precedes the output at Pin 2 by almost 0 to 100 nsec depending on the DELAY control setting. The clock module is powered by +5.8 V supplied by the PG module (from Pin 2 to Pin 1). With the INT-EXT switch in the EXT position, the clock module is disconnected from the PG module. The clock module is functioning properly if:

a) 0.1 usec TTL level outputs are observed at Pins 2 and 3.
b) The PRF of the outputs can be varied over the range of 1 KHz to 1 MHz using the PRF and PRF RANGE controls.
c) The relative delay between the Pin 2 and 3 outputs can be varied by at least 500 nsec by the DELAY control.

The sealed clock module must be returned to Avtech for repair or replacement if the above conditions are not observed.

Schroff 02.19.91