

AVTECH ELECTROSYSTEMS LTD.

NANOSECOND WAVEFORM ELECTRONICS
ENGINEERING . MANUFACTURING

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INSTRUCTIONS

Model AVM-1-IBM-1 Pulse Generator

S.N.:

Obsolete (Nov. 23/84)

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been disassembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

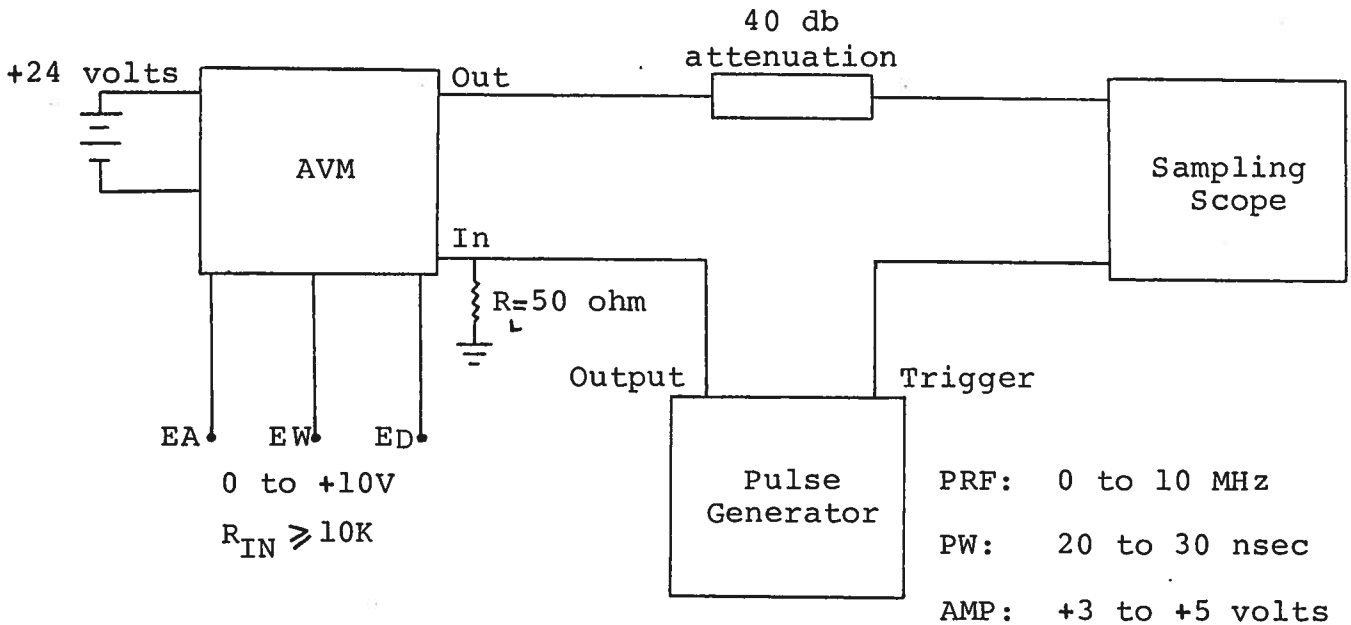
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MODEL AVM PULSE GENERATOR TEST ARRANGEMENT



Notes:

- 1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed ten gigahertz.
- 2) The use of 40 db attenuator will insure a peak input signal to the sampling scope of less than one volt.
- 3) In general, the source pulse generator trigger delay control should be set in the 0.1 to 1.0 usec range.

- 4) When testing using a general purpose 50 ohm laboratory pulse generator as the input trigger signal source, the input signal should be applied via a 50 ohm feed-through load or alternatively, the input to the AVM unit should be shunted with a 50 ohm resistor. This will prevent reflection (and degradation of the input pulse waveform) caused by the high impedance at the IN port. However, when triggering from a TTL source, no 50 ohm feed through load or resistor is necessary but lead length should be as short as possible. High-speed TTL Schottky logic is recommended for the driving circuitry.
- 5) The input trigger pulse width should be in the range of 20 to 30 nsec. WARNING: The Model AVM may fail if the input pulse width exceeds 40 nsec. The use of an input pulse width of less than 20 nsec may result in a degradation of the output waveform but will not damage the unit.
- 6) The output pulse amplitude (0 to 5 volts), pulse width (0 to 6 nsec) and relative propagation delay (0 to 5 nsec) are all controlled by DC voltages (0 to +10V, $R_{IN} \geq 10K$) applied to the back panel EA (amplitude), EW (pulse width) and ED (pulse delay) solder terminals (see Fig. 1).
- 7) The unit provides a positive output pulse at the OUT P SMA port. To obtain a negative output pulse, a short length of 80 mil semi-rigid cable is connected between the OUT P port and the IN N port. A negative pulse is then obtained at the OUT N port.
- 8) To DC offset the output pulse connect a DC power supply set to the required DC offset value to the back panel OS terminals ($\pm 50V$).
- 9) The output amplitude pulse width and PRF are inter-related. It is recommended that the following sequence be used:
 - a) Set PRF
 - b) Set output amplitude
 - c) Set pulse width

