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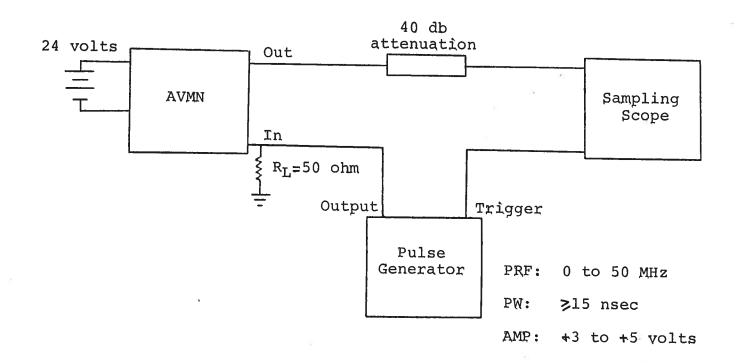CANADA K2C 3H4
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INSTRUCTIONS

MODEL AVMN-3A PULSE GENERATOR

S.N.:

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

MODEL AVMN PULSE GENERATOR TEST ARRANGEMENT

24 volts

AVMN

Out

40 db attenuation

Sampling Scope

In

R_L=50 ohm

Output

Trigger

Pulse Generator

PRF: 0 to 50 MHz

PW: ≥15 nsec

AMP: +3 to +5 volts

Notes:

1)   The bandwidth capability of components and instruments
     used to display the pulse generator output signal
     (attenuators, cables, connectors, etc.) should exceed
     ten gigahertz.

2)   The use of 40 db attenuator will insure a peak input
     signal to the sampling scope of less than one volt.

3)   In general, the source pulse generator trigger delay
     control should be set in the 0.1 to 1.0 usec range.*

4)   When testing using a general purpose 50 ohm laboratory
     pulse generator as the input trigger signal source, the
     input signal should be applied via a 50 ohm feed-through
     load or alternatively, the input to the AVMN unit should
     be shunted with a 50 ohm resistor.   This will prevent
     reflection (and degradation of the input pulse waveform)
     caused by the high impedance at the IN port. However,
     when triggering from a TTL source, no 50 ohm
     feed-through load or resistor is necessary but lead
     length should be as short as possible. High-speed TTL
     Schottky logic is recommended for the driving circuitry.

5)   The input trigger pulse width should be greater than 15
     nsec and less than one half of the pulse repetition
     frequency period. The unit triggers on the leading edge
     of the input trigger signal.

6)   The output pulse width is controlled by means of the
     one-turn potentiometer (PW).   The pot should initially
     be set maximum clockwise and the pulse width adjusted
     using an oscilloscope.

7)   The output pulse amplitude is controlled by means of the
     one-turn potentiometer (AMP).   The pulse width may
     change by several nanoseconds as the output amplitude is
     reduced from maximum to minimum.   Therefore it is
     convenient to first set the desired amplitude and then
     set the desired pulse width. Rotation of the PW pot
     causes the position of the falling edge of the pulse to
     change.

8)   Some properties of the output pulse may change as a
     function of the amplitude pot   setting.   For some
     demanding applications, it may be desirable to use a
     combination of external attenuators and the amplitude
     pot to achieve the desired output amplitude.

9)   The rise time and overshoot are controlled by the one
     turn TR pot.   Clockwise rotation of the TR pot tends to
     decrease rise time and increase overshoot.

10) The AVMN output pulse position or delay can be varied for up to 5 nsec by means of the delay (DELAY) control. Rotating the delay control clockwise increases the delay. If the full 5 nsec delay cannot be achieved then the input pulse width should be increased by a few nanoseconds. (option).

* The stability of the display on some sampling scopes is very sensitive to this delay, particularly at high PRF (eg. 10 to 50 MHz). If necessary, consult your sample scope instructions manual for the proper triggering method.

11) WARNING: Model AVMN may fail if triggered at a PRF greater than 50.0 MHz.

12) The Model AVMN pulse generator can withstand an infinite VSWR on the output port.

13) To DC offset the output pulse connect a DC power supply set to the required DC offset value to the terminals marked O.S. The maximum attainable DC offset voltage is 50 volts.

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