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INSTRUCTIONS

MODEL AVMP-3-C-M1 PULSE GENERATOR

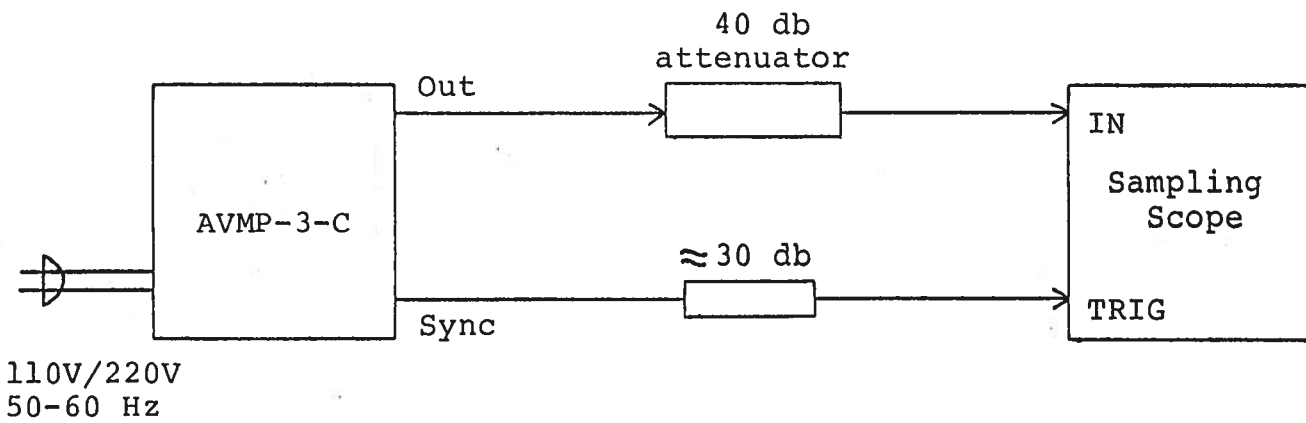
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WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been disassembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

Fig. 1

PULSE GENERATOR TEST ARRANGEMENT



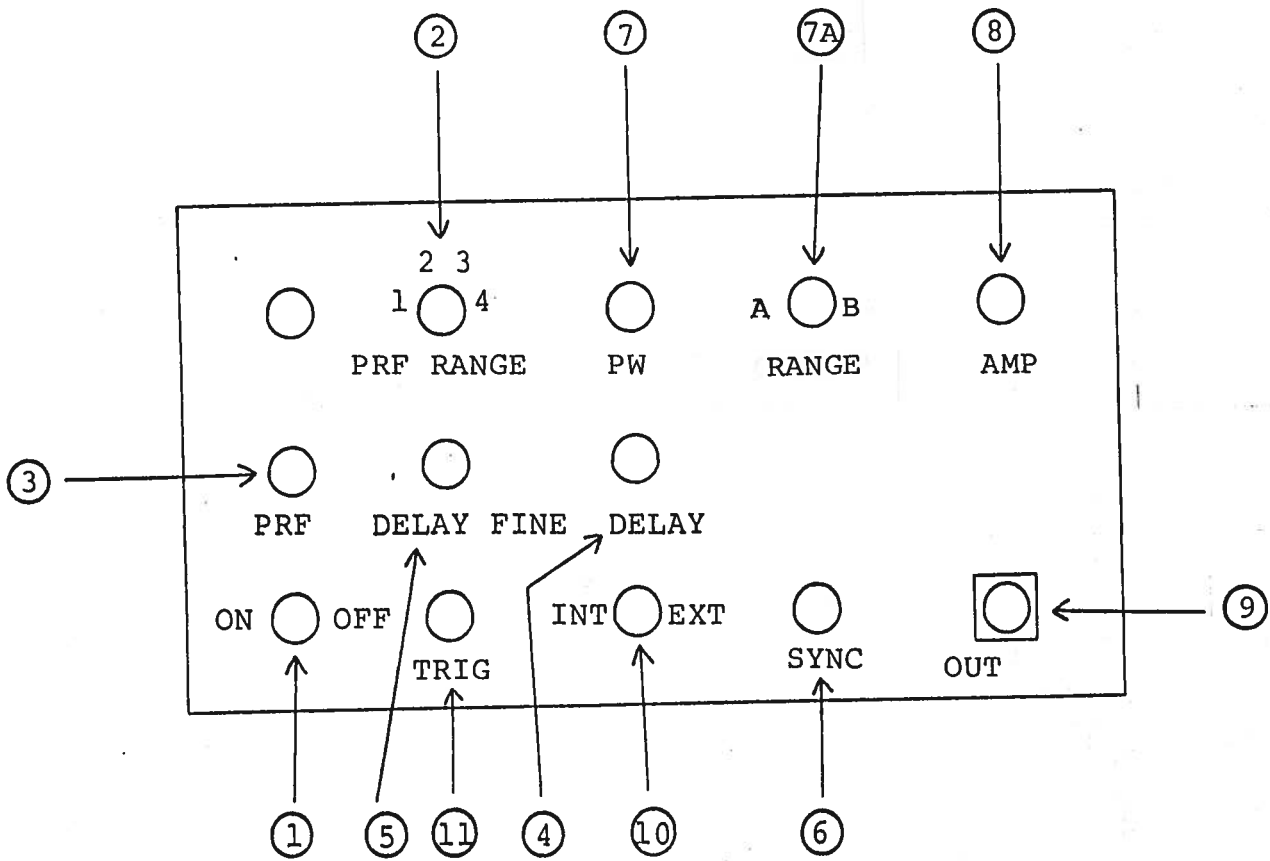
Notes:

- 1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed ten gigahertz.
- 2) The use of 40 db attenuator at the sampling scope vertical input channel will insure a peak input signal to the sampling scope of less than one volt.
- 3) The sync output channel provides TTL level signals. To avoid overdriving the TRIG input channel of some sampling scopes, a 30 db attenuator should be placed at the input to the sampling scope trigger channel.
- 4) To obtain a stable output display the PRF control on the front panel should be set mid-range while the PRF range switch may be in either range. The front panel TRIG toggle switch should be in the INT position. The front panel DELAY controls and the scope triggering controls are then adjusted to obtain a stable output. The scope may then be used to set the desired PRF by rotating the PRF control and by means of the PRF range switch.
- 5) The output pulse width is controlled by means of the front panel one turn PW control and the two position range switch. The one turn control should initially be set maximum clockwise and the pulse width adjusted using an oscilloscope. Position A of the range switch provides pulse widths in the range of 0.3 to 7.0 nsec while position B covers the range of 7 to 100 nsec.
- 6) The output pulse amplitude is controlled by means of the front panel one turn AMP control. The pulse width may change by several nanoseconds as the output amplitude is reduced from maximum to minimum. Therefore it is convenient to first set the desired amplitude and then set the desired pulse width. Rotation of the PW pot causes the position of the falling edge of the pulse to change.
- 7) Some properties of the output pulse may change as a function of the amplitude pot setting. For some demanding applications, it may be desirable to use a combination of external attenuators and the amplitude pot to achieve the desired output amplitude.
- 8) To DC offset the output pulse connect a DC power supply set to required DC offset value to the back panel terminals marked O.S. The maximum attainable DC offset voltage is ± 50 volts.

- 9) For units with the OT offset option, the output DC offset level is varied from -5 to +5V (to 50 ohm) by the front panel OFFSET one turn control. The DC offset may be turned off using the rear panel OS ON-OFF toggle switch. (OT option).
- 10) An external clock may be used to control the output PRF of the AVMP unit by setting the front panel TRIG toggle switch in the EXT position and applying a 0.2 usec (approx) TTL level pulse to the TRIG BNC connector input. For operation in this mode, the scope time base must also be triggered by the external clock rather than from the SYNC output.
- 11) The monitor output (-M) provides a 20 db attenuated coincident replica of the main output. (option).
- 12) To voltage control the output pulse width, remove the jumper wire between banana plugs A and B on the back panel and apply 0 to +10V to connector B ($R_{IN} \gg 10K$). (EW option).
- 13) To voltage control the output amplitude, remove the jumper wire between banana plugs A and B on the back panel and apply 0 to +10V to connector B ($R_{IN} \gg 10K$). (EA option).
- 14) To invert the output of the AVMP unit, connect the AVX-3-T unit to the OUT port. An inverted pulse is then obtained at the OUT port of the AVX-3-T unit. To offset the inverted pulse, apply the required DC level to the DC terminal of the AVX-3-T unit. To offset the non-inverted pulse, apply the required DC level to the OS terminals of the AVMP back panel. (PN option).

Fig. 2

FRONT PANEL CONTROLS



- (1) ON-OFF Switch. Applies basic prime power to all stages.
- (2) PRF Control. The PRF RANGE and PRF controls determine
- (3) output PRF as follows:

	PRF MIN	PRF MAX
Range 1	100 Hz	1 KHz
Range 2	1 KHz	10 KHz
Range 3	10 KHz	100 KHz
Range 4	100 KHz	1 MHz

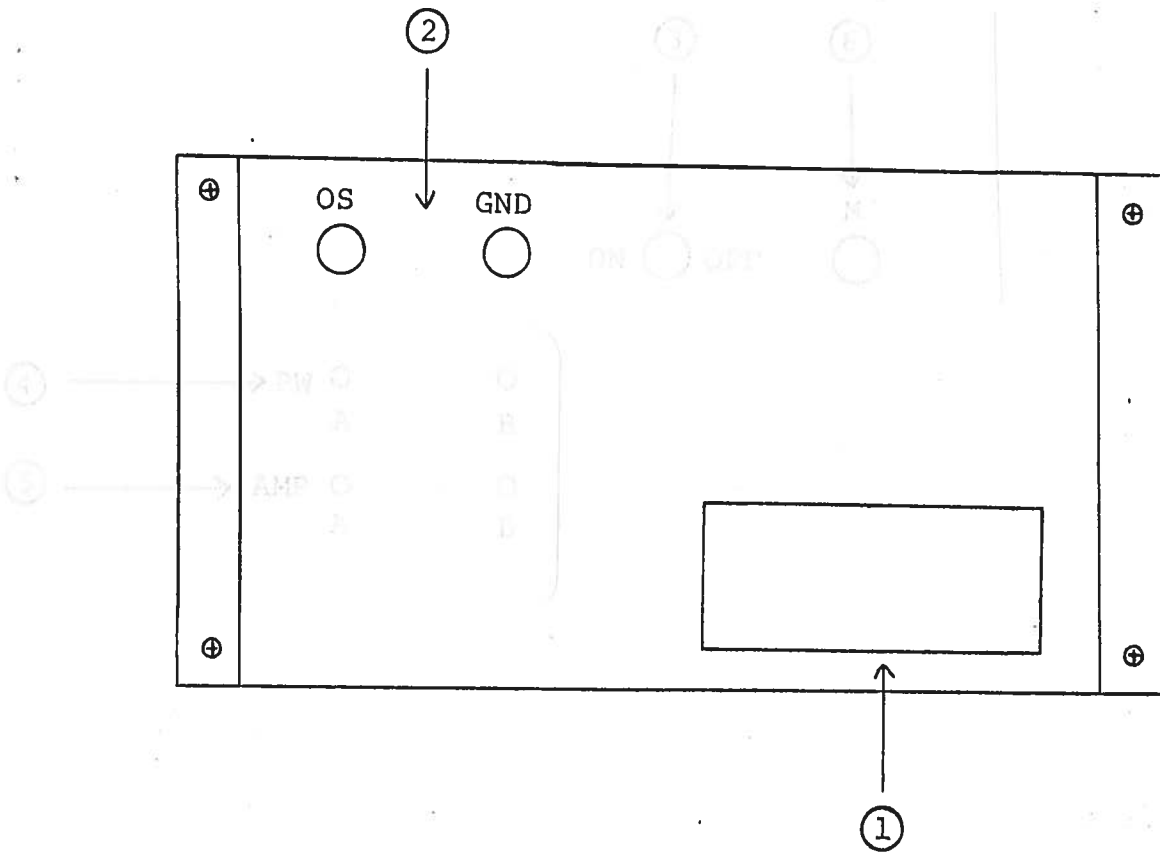
- (4) DELAY Controls. Controls the relative delay between the
- (5) reference output pulse provided at the SYNC output (6)
- and the main output (9). This delay is variable over
- the range of 0 to at least 500 nsec.
- (6) SYNC Output. This output precedes the main output (9)
- and is used to trigger the sampling scope time base.
- The output is a TTL level 100 nsec (approx) pulse
- capable of driving a fifty ohm load.
- (7) PW Control. A one turn control and two position range
- (7A) switch which vary the output pulse width as follows:

RANGE A: 0.3 to 7.0 nsec
RANGE B: 7.0 to 100 nsec

- (8) AMP Control. A one turn control which varies the output
- pulse amplitude.
- (9) OUT. SMA connector provides output to 50 ohm load.
- (10) EXT-INT Control. With this toggle switch in the INT
- position, the PRF of the AVMP unit is controlled via an
- internal clock which in turn is controlled by the PRF
- controls. With the toggle switch in the EXT position,
- the AVMP unit requires a 0.2 usec TTL level pulse
- applied at the TRIG input in order to trigger the output
- stages. In addition, in this mode, the scope time base
- must be triggered by the external trigger source.
- (11) TRIG Input. The external trigger signal is applied at
- this input when the EXT-INT toggle switch is in the EXT
- position.

Fig. 3

BACK PANEL CONTROLS

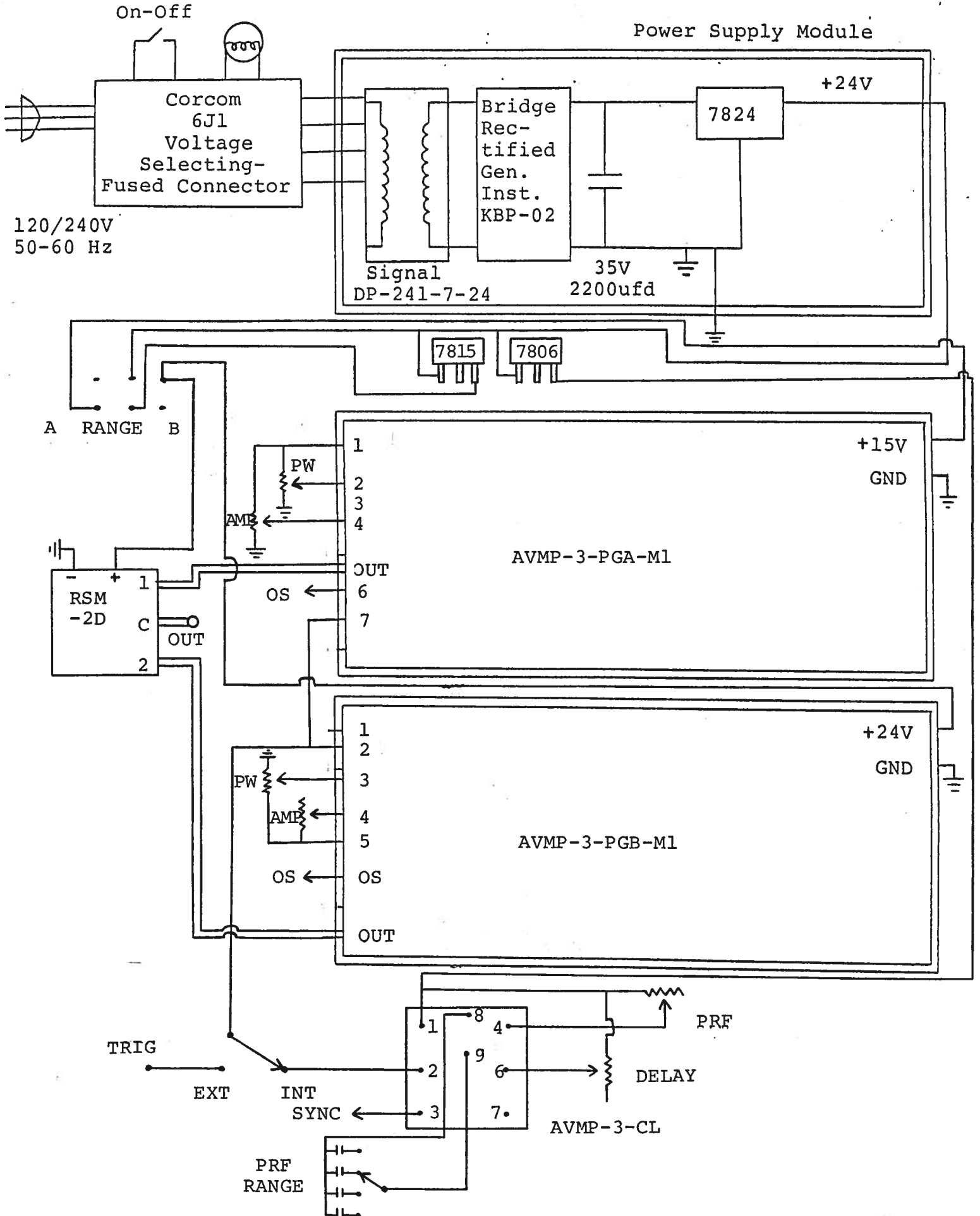


- (1) FUSED CONNECTOR, VOLTAGE SELECTOR. The detachable power cord is connected at this point. In addition, the removable cord is adjusted to select the desired input operating voltage. The unit also contains the main power fuse.

- (2) DC OFFSET Input. To DC offset the output pulse, connect a DC power supply set to the desired offset value to these terminals. The maximum allowable DC offset voltage is ± 50 volts.

Fig. 4

SYSTEM BLOCK DIAGRAM



SYSTEM DESCRIPTION AND REPAIR PRODECURE

The AVMP-3-C consists of two pulse generator modules (AVMP-3-PGA, -PGB), a clock module (AVMP-CL) and a power supply board which supplies +24 volts (600 mA max) to the pulse generator modules. In the event that the unit malfunctions, remove the instrument cover by removing the four Phillips screws on the back panel of the unit. The top cover may then be slid off. Measure the voltage at the +24 V pin of the PG module. If this voltage is substantially less than +24 volts, unsolder the line connecting the power supply and PG modules and connect 100 ohm 10 W load to the PS output. The voltage across this load should be about +24 V DC. If this voltage is substantially less than 24 volts the PS module is defective and should be repaired or replaced. If the voltage across the resistor is near 24 volts, then the PG module should be replaced or repaired. The sealed PG module must be returned to Avtech for repair (or replacement). The clock module provides a 0.1 usec TTL level trigger pulse at Pin 2 to trigger the PG module and a 0.1 usec TTL level sync pulse at Pin 3 to trigger the sampling scope display device. The output at Pin 3 precedes the output at Pin 2 by almost 0 to 100 nsec depending on the DELAY control setting. The clock module is powered by +5.8 V supplied by the PG module (from Pin 2 to Pin 1). With the INT-EXT switch in the EXT position, the clock module is disconnected from the PG module. The clock module is functioning properly if:

- a) 0.1 usec TTL level outputs are observed at Pins 2 and 3.
- b) The PRF of the outputs can be varied over the range of 1 KHz to 1 MHz using the PRF and PRF RANGE controls.
- c) The relative delay between the Pin 2 and 3 outputs can be varied by at least 500 nsec by the DELAY control.

The sealed clock module must be returned to Avtech for repair or replacement if the above conditions are not observed.

Schroff

05.12.86

-OT

-M

-EW

-EA

-PN