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INSTRUCTIONS

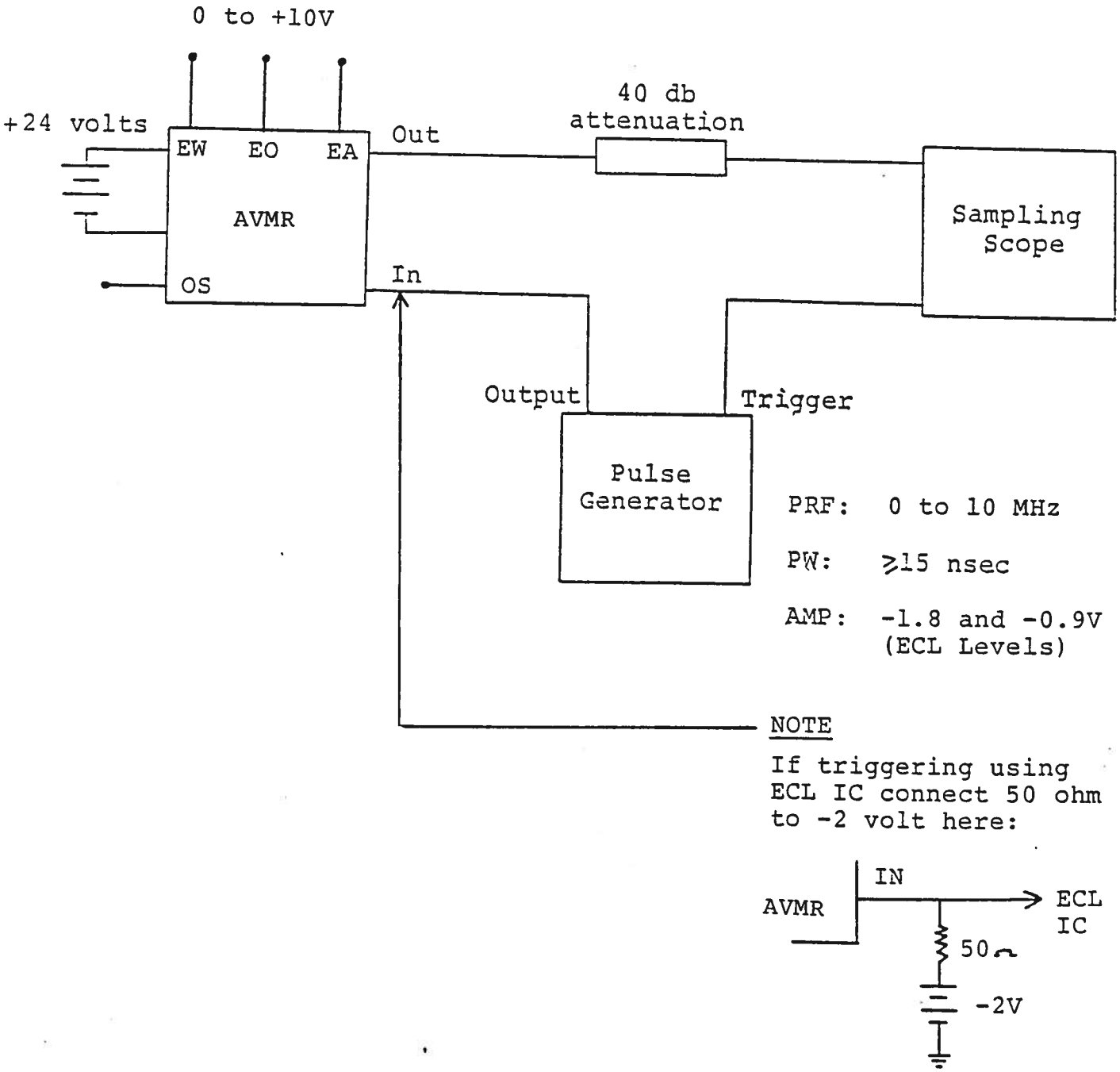
MODEL AVMR-1-TRF-EW-EA-EO-ECL-M1 PULSE GENERATOR

S.N.:

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

MODEL AVMR PULSE GENERATOR TEST ARRANGEMENT



Notes:

1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed 10 gigahertz.

2) The use of 40 db attenuator will insure a peak input signal to the sampling scope of less than one volt.

3) In general, the source pulse generator trigger delay control should be set in the 0.1 to 1.0 usec range.

4) The AVMR requires an ECL trigger signal (-0.9 and -1.8 volts). If triggered directly from an ECL IC, the input to the AVMR should be shunted by 50 ohms terminated in -2 volts.

5) The input trigger pulse width should be greater than 15 nsec and less than one half of the pulse repetition frequency period. The unit triggers on the leading edge of the input trigger signal.

6) WARNING: Model AVMR may fail if triggered at a PRF greater than 10.0 MHz.

7) The output pulse width and amplitude are each controlled by 0 to +10 volts applied to the EW and EA solder terminals ($R_{IN} \geqslant 10K$).

8) The output DC offset is controlled by 0 to +10 volts applied to the EO solder terminal when the EO switch is in the ON position. The output offset is -5 volts when OV is applied and increases to +5 volts when +10 volts is applied. When the EO switch is in the OFF position, the internally generated offset is inactive but a DC offset can be applied by connecting a desired potential to the rear panel OS solder terminal.

9) With the TR switch in the L position, the unit provides an output rise time of 150 psec. With the TR switch in the H position, the rise time is about 1 nsec.

10) The TF switch provides a fall time of 150 psec when in the L position and a fall time of 1 nsec when in the H position.

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