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INSTRUCTIONS

MODEL AVMR-1-C-N-ED-EA-EF-LA2 PULSE GENERATOR

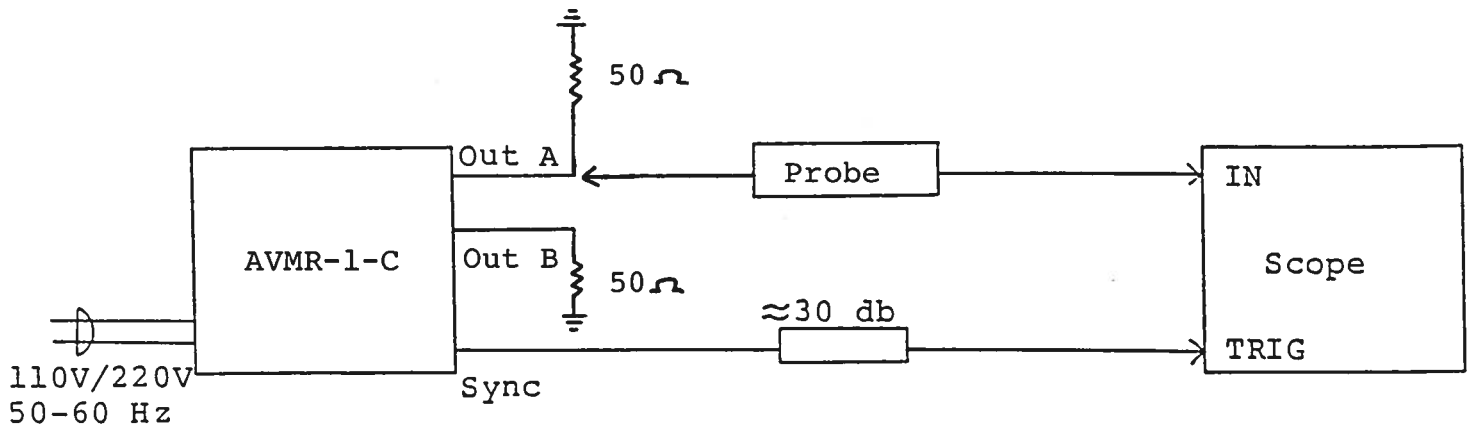
S.N.:

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been disassembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

Fig. 1

PULSE GENERATOR TEST ARRANGEMENT



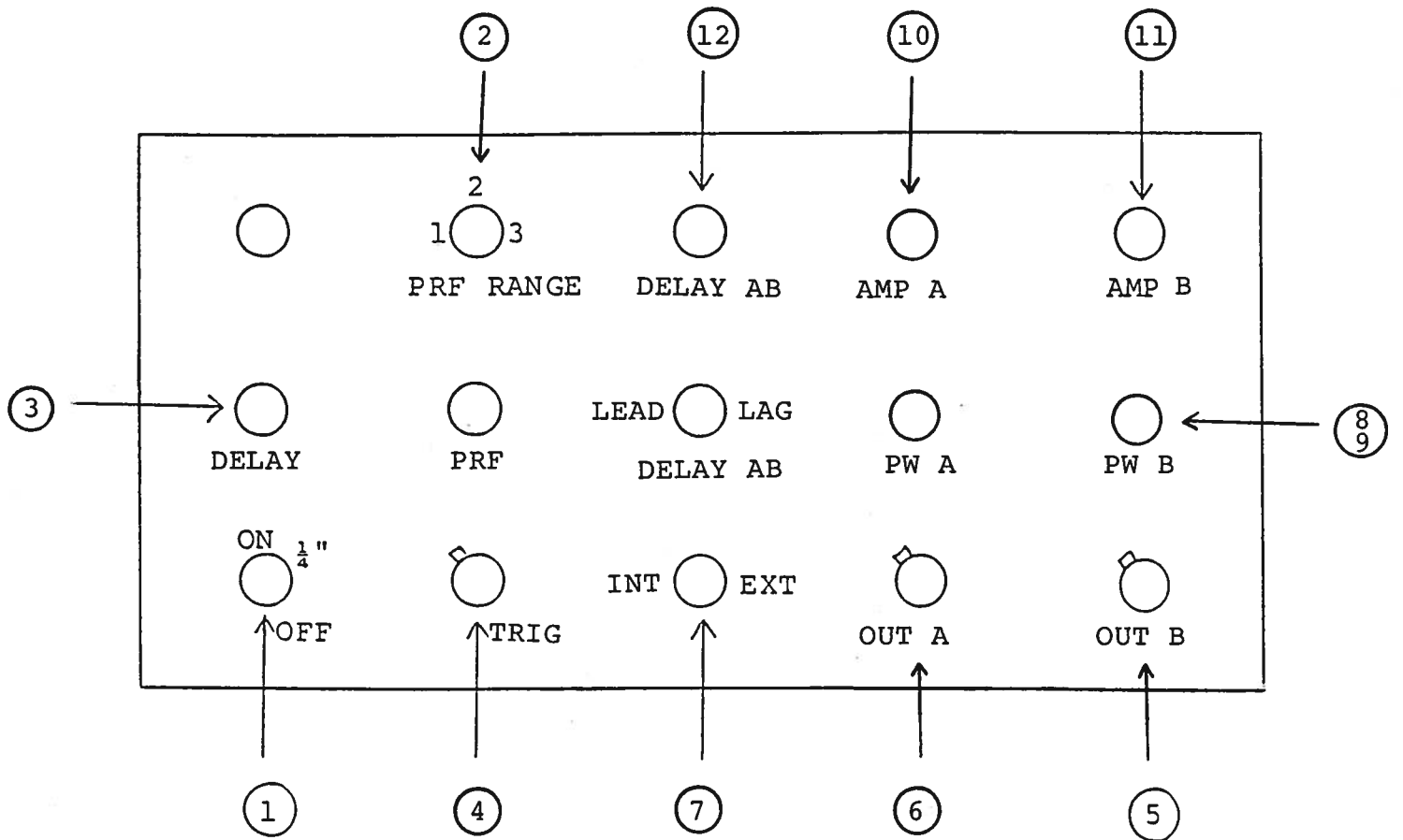
Notes:

- 1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed 500 MHz.
- 2) The use of 60 db attenuator at the scope vertical input channel will insure a peak input signal to the scope of less than one volt (necessary only if sampling scope used). If a high impedance real time scope is used, the pulse generator should be terminated using a shunt 50 ohm resistor.
- 3) The sync output channel provides TTL level signals. To avoid overdriving the TRIG input channel of some scopes, a 30 db attenuator should be placed at the input to the scope trigger channel.
- 4) To obtain a stable output display the PW and PRF controls on the front panel should be set mid range. The front panel TRIG toggle switch should be in the INT position. The DELAY controls and the scope triggering controls are then adjusted to obtain a stable output. The scope may then be used to set the desired PRF by rotating the PRF controls.
- 5) The output pulse widths are controlled by means of the front panel one turn PW controls, PWA and PWB.
- 6) The output pulse amplitudes are controlled by means of the front panel one turn AMP controls (AMP A and AMP B). To voltage control the output, set the rear panel switches in the EXT position and apply 0 to +10 volts between terminal A and ground ($R_{IN} > 10K$).
- 7) The PRF is controlled by the three position PRF range switch and the one turn PRF control. To voltage control the PRF within each range, set the rear panel FREQ switch in the EXT position and apply 0 to +10 volts between terminal A and ground.
- 8) An external clock may be used to control the output PRF of the AVR unit by setting the front panel TRIG toggle switch in the EXT position and applying a 0.2 usec (approx.) TTL level pulse to the TRIG BNC connector input. For operation in this mode, the scope time base must also be triggered by the external clock rather than from the SYNC output.

- 9) The relative time delay between the A output and B outputs is controlled by the DELAY AB one turn control and the DELAY AB LEAD-LAG switch. With the switch in the LEAD position output A precedes output B while with the switch in the LAG position, output A follows output B. To voltage control the relative delay, set the rear panel DELAY AB switch in the EXT position and apply 0 to +10 volts between terminal A and ground.

Fig. 2

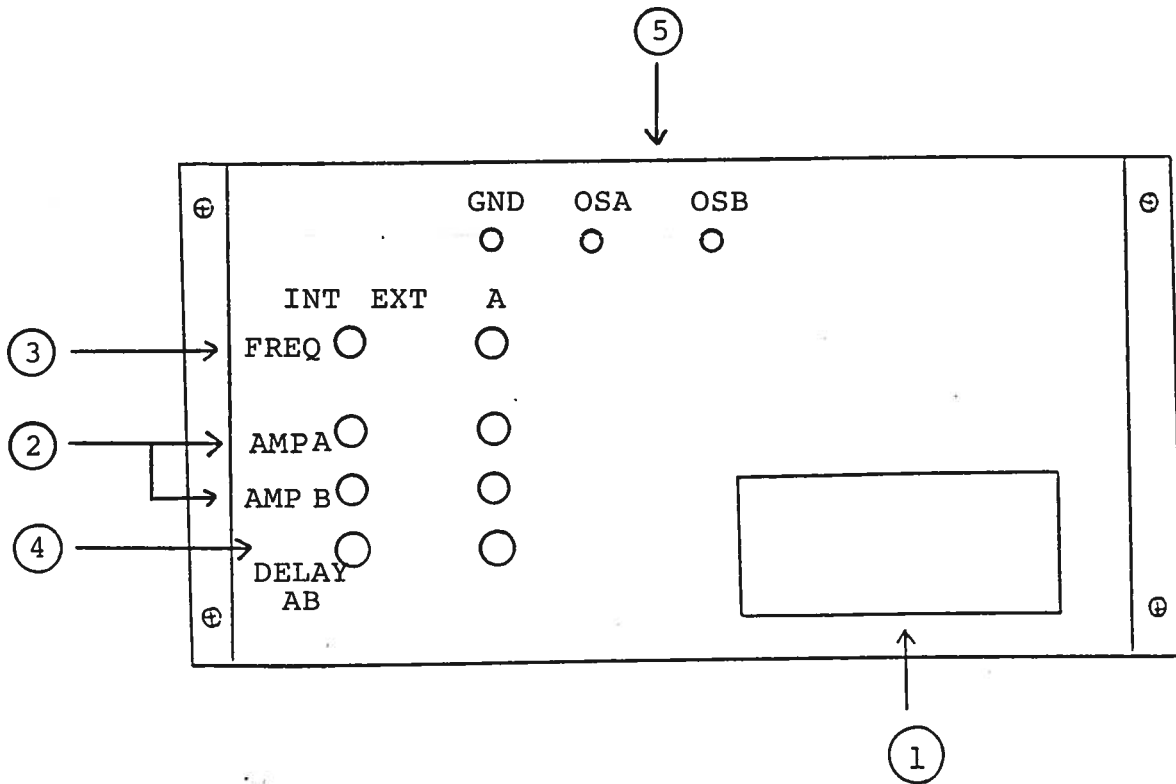
FRONT PANEL CONTROLS



- (1) ON-OFF Switch. Applies basic prime power to all stages.
- (2) PRF Control. With the PRF range switch in 1 position, PRF control will vary PRF from .05 KHz to about 0.5 KHz. With the PRF range switch in 2 position, varies PRF from about 0.5 KHz to about 5.0 KHz. With the PRF range switch in the 3 position, varies PRF from about 5 KHz to 50 KHz. The operating PRF should be set using a scope.
- (3) DELAY Control. Controls the relative delay between the reference output pulse provided at the TRIG output (4) and the main outputs (5), (6). This delay is variable over the range of 0 to about 1.0 usec.
- (4) TRIG Output. This output precedes the main output (5) and is used to trigger the scope time base. The output is a TTL level 100 nsec (approx.) pulse capable of driving a fifty ohm load. The external trigger signal is applied at this input when the EXT-INT toggle switch (7) is in the EXT position.
- (5) OUT Connector. BNC connector provides output to a fifty
- (6) ohm load.
- (7) EXT-INT Control. With this toggle switch in the INT position, the PRF of the AVMR unit is controlled via an internal clock which in turn is controlled by the PRF and PRF FINE controls. With the toggle switch in the EXT position, the AVMR unit requires a 0.2 usec TTL level pulse applied at the TRIG input in order to trigger the output stages. In addition, in this mode, the scope time base must be triggered by the external trigger source.
- (8) PW Control. A one turn control which varies the output
- (9) pulse width from 0.1 usec to 0.5 usec.
- (10) AMP Control. A one turn control which varies the output
- (11) pulse amplitude from 0 to -5V to a fifty ohm load.
- (12) The relative time delay between the A output and B outputs is controlled by the DELAY AB one turn control and the DELAY AB LEAD-LAG switch. With the switch in the LEAD position output A precedes output B while with the switch in the LAG position, output A follows output B.

Fig. 3

BACK PANEL CONTROLS



- (1) FUSED CONNECTOR, VOLTAGE SELECTOR. The detachable power cord is connected at this point. In addition, the removable cord is adjusted to select the desired input operating voltage. The unit also contains the main power fuse.
- (2) AMP. To voltage control the output amplitude, set the switch in the EXT position and apply 0 to +10 volts between terminal A and ground ($R_{IN} > 10K$). (option).
- (3) FREQ. To voltage control the output PRF, set the switch in the EXT position and apply 0 to +10 volts between terminal A and ground ($R_{IN} > 10K$). (option).
- (4) DELAY AB. To voltage control the relative delay between A and B outputs, set the DELAY AB switch in the EXT position and apply 0 to +10 volts between terminal A and ground.
- (5) OSA, OSB. To DC offset the output pulse, connect a DC power supply set to the desired offset value to these terminals. The maximum allowable DC offset voltage is +50 volts, max current ± 100 mA.

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1. The first part of the document discusses the general principles of the proposed system. It outlines the objectives and the scope of the project, emphasizing the need for a comprehensive and integrated approach to the problem at hand.

2. The second part of the document provides a detailed description of the system's architecture. It details the various components and their interactions, highlighting the modular and scalable nature of the design.

3. The third part of the document discusses the implementation and testing of the system. It describes the development process, the testing methodology, and the results of the experiments, demonstrating the system's effectiveness and reliability.

4. The fourth part of the document concludes the report by summarizing the key findings and providing recommendations for future work. It emphasizes the importance of continued research and development in this area.

5. The final part of the document includes a list of references and a list of figures. The references cite the key literature sources used in the research, and the figures provide visual representations of the system's performance and architecture.