# AVTECH ELECTROSYSTEMS LTD.

NANOSECOND WAVEFORM ELECTRONICS
ENGINEERING . MANUFACTURING

P.O. BOX 265
OGDENSBURG
NEW YORK
13669
(315) 472-5270

BOX 5120 STN. "F"
OTTAWA, ONTARIO
CANADA K2C 3H4
(613) 226-5772
TELEX 053-4591


## INSTRUCTIONS

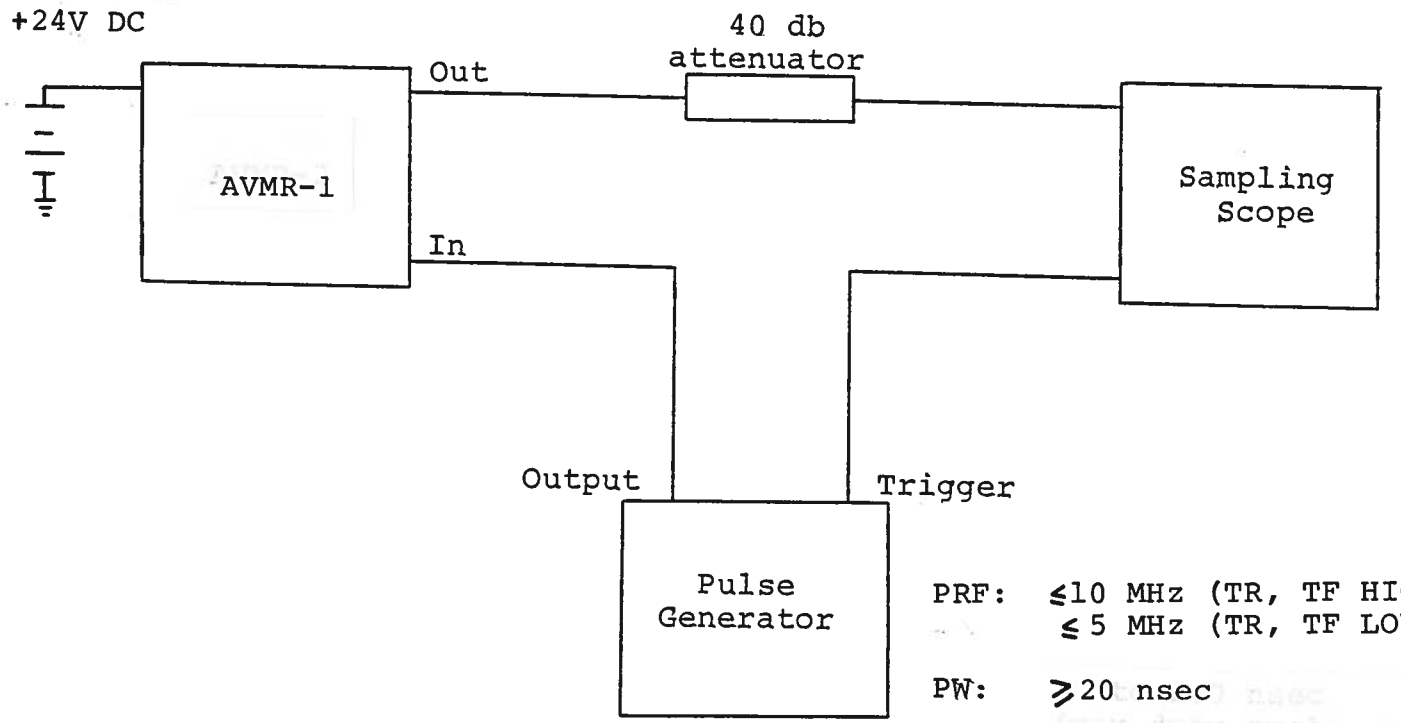
## MODEL AVMR-1-TRF-EW PULSE GENERATOR

S.N.:

# WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

# MODEL AVMR-2 PULSE GENERATOR TEST ARRANGEMENT




PRF: ≤10 MHz (TR, TF HIGH)
≤ 5 MHz (TR, TF LOW)

PW: ≥20 nsec

AMP: +3 to +5 volts
(TTL Levels)

Notes:

1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed one gigahertz.

2) The use of 40 db attenuator will insure a peak input signal to the sampling scope of less than one volt.

3) When triggering the AVMR-1 from a high speed lab pulse generator it may be necessary to shunt the input to the AVMR-1 by a 50 ohm resistor to eliminate reflection which may interfere with the operation of the lab pulse generator.

4) In general, the source pulse generator trigger delay control should be set in the 0.1 to 1.0 usec range. Other settings should be as shown in the above diagram.

5) WARNING: Model AVMR-1 may fail if triggered at a PRF greater than 10 MHz or if the duty cycle exceeds 20% or if the PW exceeds 200 nsec.

6) The output amplitude is controlled by means of the one turn potentiometer (AMP).

7) The output pulse width is controlled by means of a DC voltage (0 to +10V, $R_{IN} \geq 10K$) applied to the PW solder terminals.

8) With the TR switch in the L position, the unit provides an output rise time of 150 psec. With the TR switch in the H position, the rise time is about 1 nsec.

9) The TF switch provides a fall time of 150 psec when in the L position and a fall time of 1 nsec when in the H position.

10) The PRF should not exceed 5 MHz when either the TR or TF switches are in the LOW position.

11) The required output DC offset voltage is applied to the rear panel OS solder terminals ($\pm$50 volts, 100 mA max).

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-OS