AVTECH ELECTROSYSTEMS LTD.

NANOSECOND WAVEFORM ELECTRONICS
ENGINEERING - MANUFACTURING

P.O. BOX 265
OGDENSBURG
NEW YORK
13669
(315) 472-5270

BOX 5120 STN. "F"
OTTAWA, ONTARIO
CANADA K2C 3H4
(613) 226-5772
TELEX 053-4591

INSTRUCTIONS

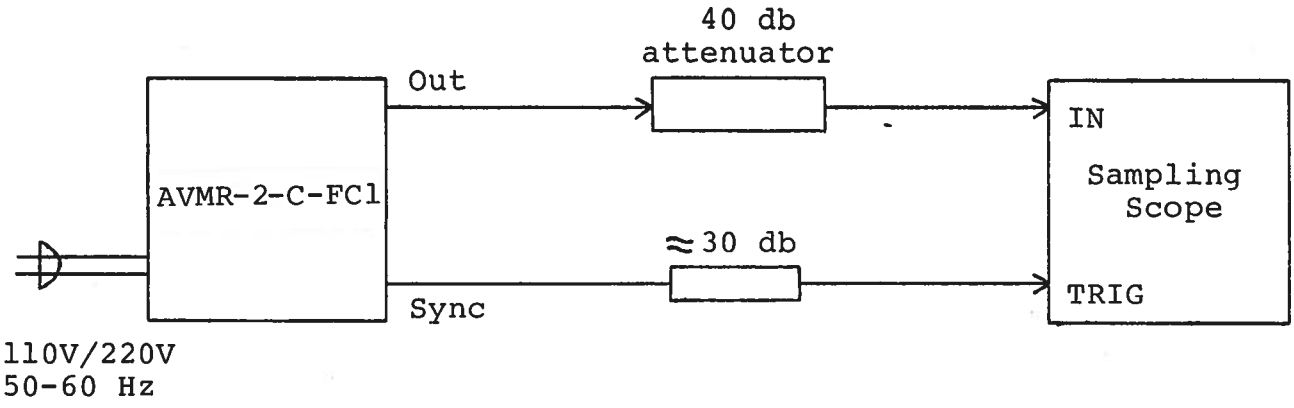
MODEL AVMR-2-C-FC1 PULSE GENERATOR

S.N.:

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

Fig. 1 PULSE GENERATOR TEST ARRANGEMENT



Notes:

1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed ten gigahertz.

2) The use of 40 db attenuator at the sampling scope vertical input channel will insure a peak input signal to the sampling scope of less than one volt.

3) The sync output channel provides TTL level signals. To avoid overdriving the TRIG input channel of some sampling scopes, a 30 db attenuator should be placed at the input to the sampling scope trigger channel.

4) To obtain a stable output display the PRF control on the front panel should be set mid-range while the PRF range switch may be in either range. The front panel TRIG toggle switch should be in the INT position. The front panel DELAY controls and the scope triggering controls are then adjusted to obtain a stable output. The scope may then be used to set the desired PRF by rotating the PRF control and by means of the PRF range switch.

5) The output pulse width is controlled by means of the front panel one turn PW control and the 3 position PW RANGE switch. The PW should be set using an oscilloscope taking care not to exceed a 20% duty cycle as this may result in failure of the output switching elements. The maximum allowable output pulse width as a function of frequency is as follows:

PRF	PW MAX
1.0 MHz	200 nsec
100 KHz	2.0 usec
40 KHz or lower	5.0 usec

6) The output pulse amplitude is controlled by means of the front panel one turn AMP control. The pulse width may change by several nanoseconds as the output amplitude is reduced from maximum to minimum. Therefore it is convenient to first set the desired amplitude and then set the desired pulse width. Rotation of the PW pot causes the position of the falling edge of the pulse to change.

7) Some properties of the output pulse may change as a function of the amplitude pot setting. For some

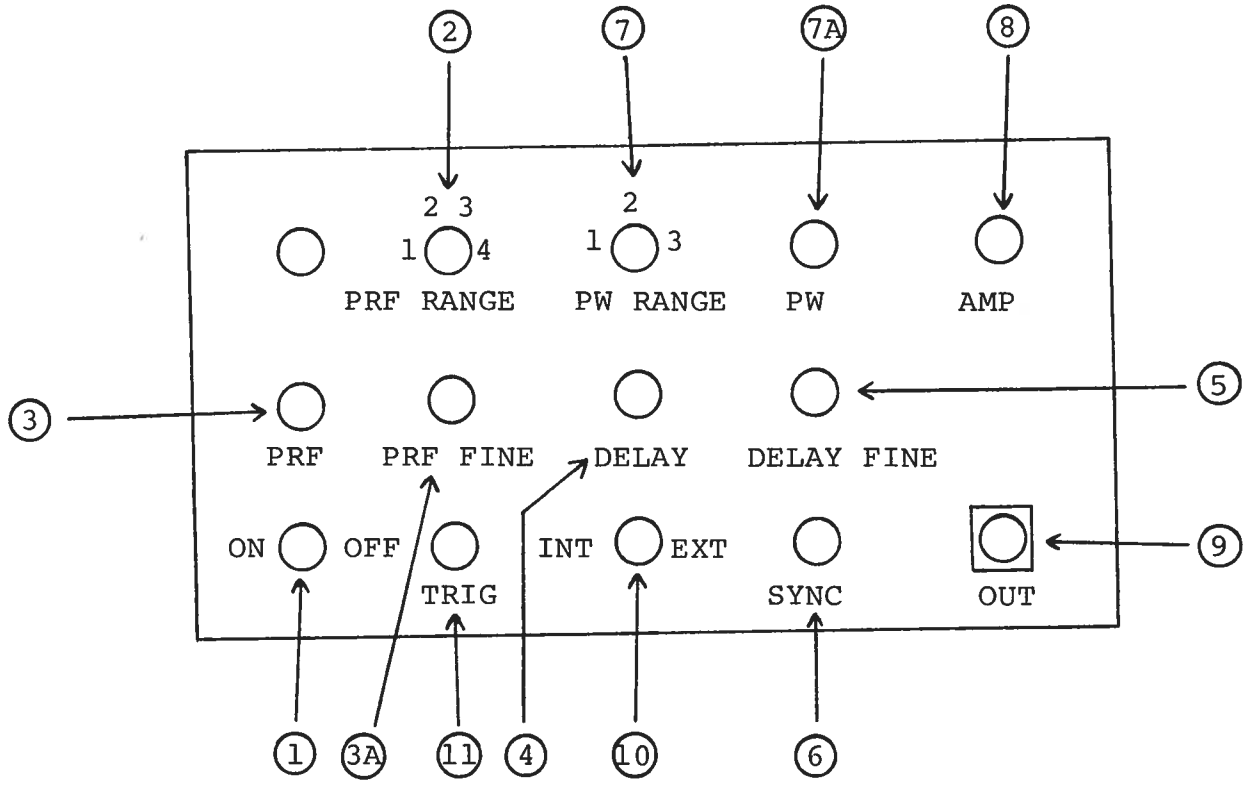
demanding applications, it may be desirable to use a combination of external attenuators and the amplitude pot to achieve the desired output amplitude.

8) To DC offset the output pulse connect a DC power supply set to required DC offset value to the back panel terminals marked O.S. The maximum attainable DC offset voltage is ±50 volts. (option).

9) An external clock may be used to control the output PRF of the AVMR unit by setting the front panel TRIG toggle switch in the EXT position and applying a 0.2 usec (approx) TTL level pulse to the TRIG BNC connector input. For operation in this mode, the scope time base must also be triggered by the external clock rather than from the SYNC output.

10) The AVMR unit is designed to operate into a 50 ohm load but will withstand an output short circuit or open circuit condition. The output transistors are field-replaceable following the instructions in the Repair Procedure Section.

Fig. 2 FRONT PANEL CONTROLS



(1) ON-OFF Switch. Applies basic prime power to all stages.

(2) PRF Control. The PRF RANGE and PRF controls determine
(3) output PRF as follows:
(3A)

	PRF MIN	PRF MAX
Range 1	150 Hz	1.5 KHz
Range 2	1.5 KHz	18 KHz
Range 3	18 KHz	164 KHz
Range 4	150 KHz	1.2 MHz

(4) DELAY Controls. Controls the relative delay between the
(5) reference output pulse provided at the SYNC output (6) and the main output (9). This delay is variable over the range of 0 to at least 1.0 usec.

(6) SYNC Output. This output precedes the main output (9) and is used to trigger the sampling scope time base. The output is a TTL level 100 nsec (approx) pulse capable of driving a fifty ohm load.

(7) PW Control. A 3 position range switch and a one turn
(7A) control which control output pulse width as follows:

	PW MIN	PW MAX
Range 1	50 nsec	720 nsec
Range 2	520 nsec	2.0 usec
Range 3	1.0 usec	5.0 usec

Extreme care must be taken not to exceed the 20% duty cycle limit of the instrument as this may result in failure of the output switching elements. The maximum allowable output pulse width as a function of frequency is as follows:

PRF	PW MAX
1.0 MHz	200 nsec
100 KHz	2.0 usec
40 KHz or lower	5.0 usec

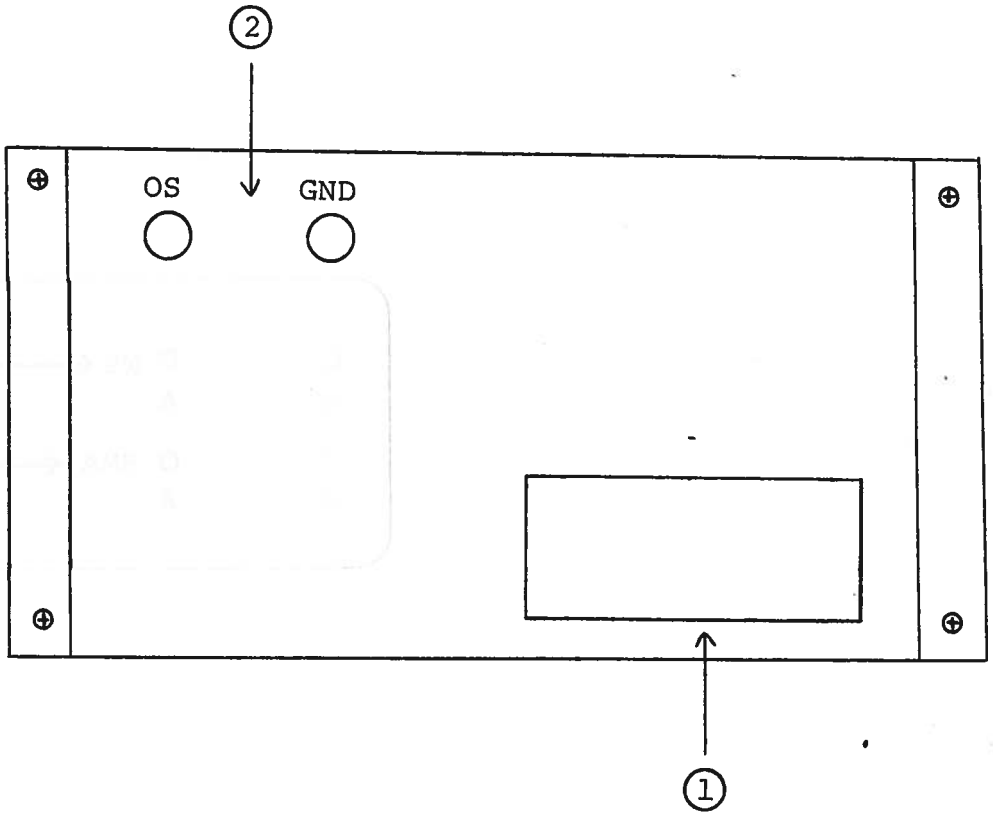
(8) AMP Control. A one turn control which varies the output pulse amplitude from 0 to -10 volts to a 50 ohm load.

(9) OUT. SMA connectors provides 0 to -10 volts to fifty ohms.

(10) EXT-INT Control. With this toggle switch in the INT position, the PRF of the AVMR unit is controlled via an internal clock which in turn is controlled by the PRF controls. With the toggle switch in the EXT position, the AVMR unit requires a 0.2 usec TTL level pulse applied at the TRIG input in order to trigger the output stages. In addition, in this mode, the scope time base must be triggered by the external trigger source.

(11) TRIG Input. The external trigger signal is applied at this input when the EXT-INT toggle switch is in the EXT position.

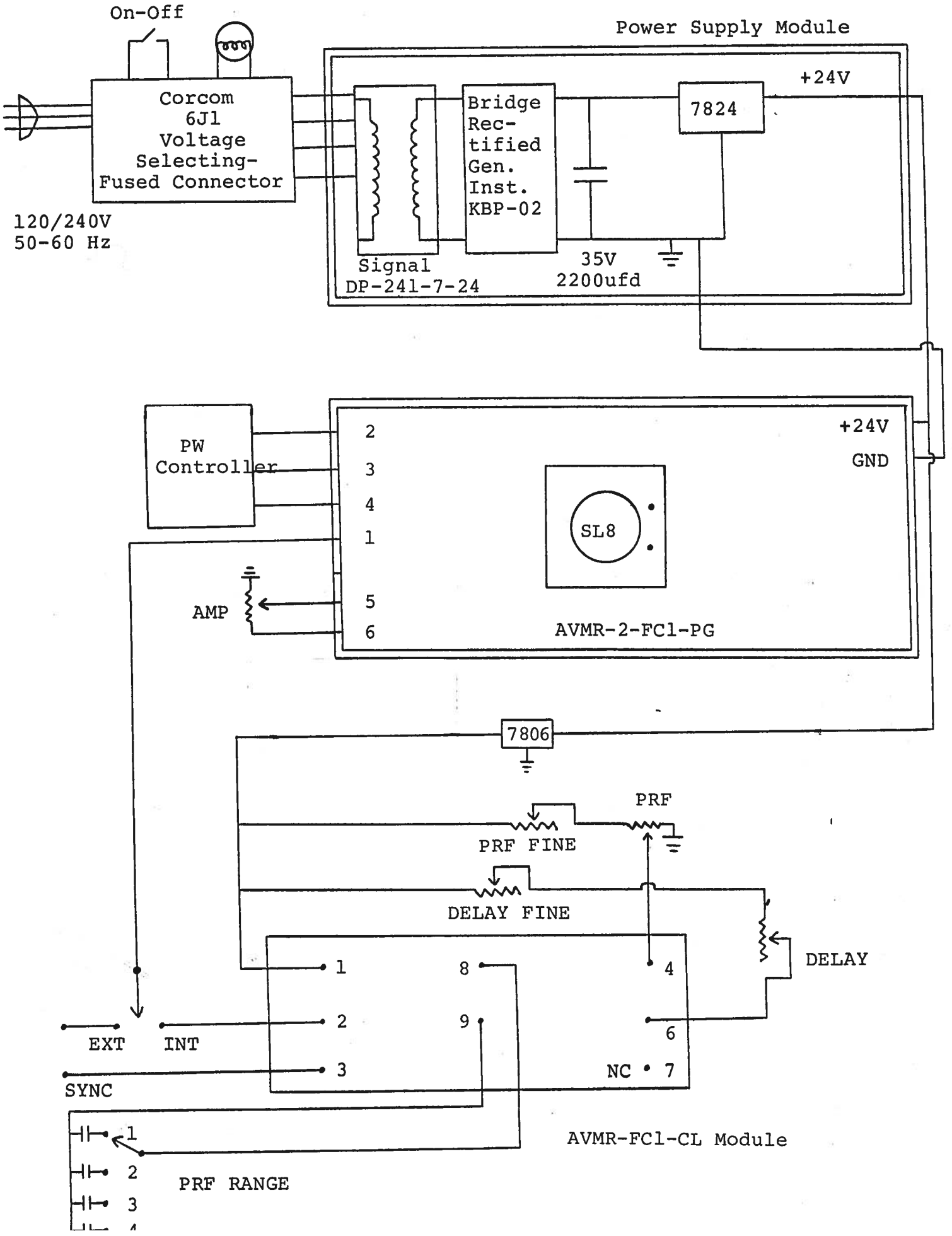
Fig. 3 BACK PANEL CONTROLS



(1) FUSED CONNECTOR, VOLTAGE SELECTOR. The detachable power cord is connected at this point. In addition, the removable cord is adjusted to select the desired input operating voltage. The unit also contains the main power fuse.

(2) DC OFFSET Input. To DC offset the output pulse, connect a DC power supply set to the desired offset value to these terminals. The maximum allowable DC offset voltage is ±50 volts, 250 mA.

Fig. 4 SYSTEM BLOCK DIAGRAM



SYSTEM DESCRIPTION AND REPAIR PROCEDURE

The AVMR-2-C-FC1 consists of the following basic modules:

1) AVMR-2-FC1-PG pulse generator module
2) AVMR-FCL-CL clock module
3) +24V power supply board

The modules are interconnected as shown in Fig. 4. The clock module controls the output PRF and the relative delay between the main output and the SYNC outputs. The PG pulse generator module generates the output pulse. In the event of an instrument malfunction, it is most likely that some of the output switching elements (SL8) may have failed due to a high duty cycle condition. The switching elements may be accessed by removing the cover plate on the bottom side of the instrument. NOTE: First turn off the prime power. The elements may be removed from their sockets by means of a needle nosed pliers. The SL8 is a selected VMOS power transistor in a TO 220 packages and may be checked on a curve tracer. If defective, replacement units should be ordered directly from Avtech. When replacing the SL8 switching elements, take care to insure that the short lead (of the three leads) is adjacent to the black dot on the chassis. If the switching elements are not defective, then the four Phillips screws on the back panel should be removed. The top cover may then be slid off and operation of the clock and power supply modules should be checked. The clock module is functioning properly if:

a) 0.1 usec TTL level outputs are observed at Pins 2 and 3.

b) The PRF of the outputs can be varied over the range of 0.1 KHz to 1.0 MHz using the PRF, PRF FINE and PRF RANGE controls.

c) The relative delay between the Pin 2 and 3 outputs can be varied by at least 1 usec by the DELAY controls.

The sealed clock module must be returned to Avtech for repair or replacement if the above conditions are not observed. The power supply board generates +24V DC to power the other modules. If the voltage is less than +24V, turn off the prime power and unsolder the lead from the 7824 regulator chip on the power supply board. Solder a 100 ohm 5 watt resistor to the 7824 output to ground and turn on the prime power. A voltage of +24 volts should be read. If the voltage is less then the power supply board is defective and should be repaired or replaced.

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