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INSTRUCTIONS

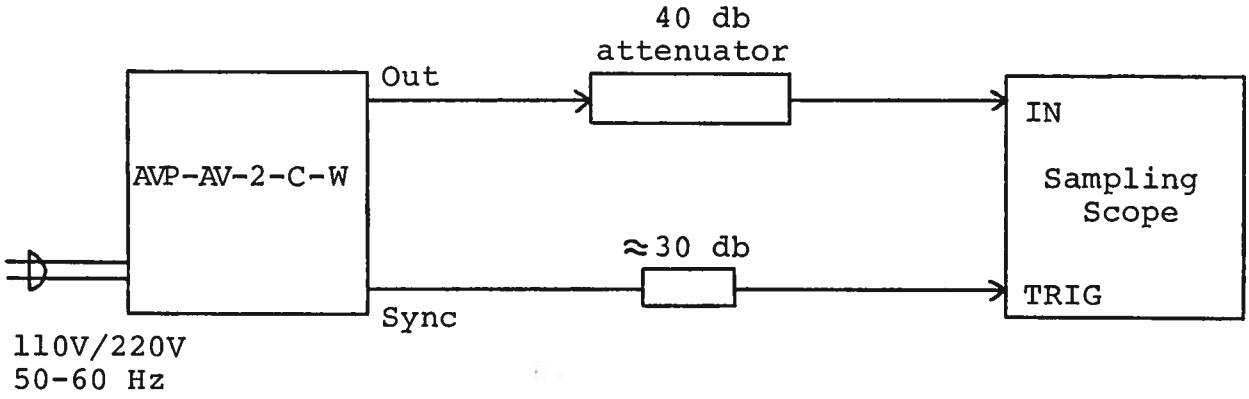
MODEL AVP-AV-2-W-C-EA-EW-EO-N-PN-MA1-ECL PULSE GENERATOR

S.N.:

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

Fig. 1 PULSE GENERATOR TEST ARRANGEMENT



Notes:

1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed ten gigahertz.

2) The use of 40 db attenuator at the sampling scope vertical input channel will insure a peak input signal to the sampling scope of less than one volt.

3) The sync output channel provides TTL level signals. To avoid overdriving the TRIG input channel of some sampling scopes, a 30 db attenuator should be placed at the input to the sampling scope trigger channel.

4) To obtain a stable output display the PRF control on the front panel should be set mid-range while the PRF range switch may be in either range. The front panel TRIG toggle switch should be in the INT position. The front panel DELAY controls and the scope triggering controls are then adjusted to obtain a stable output. The scope may then be used to set the desired PRF by rotating the PRF control and by means of the PRF range switch.

5) The output pulse width is controlled by means of the front panel ten turn PW control. The control should initially be set maximum counter clockwise and the pulse width adjusted using an oscilloscope.

6) The output pulse amplitude is controlled by means of the front panel ten turn AMP control. The pulse width may change by several nanoseconds as the output amplitude is reduced from maximum to minimum. Therefore it is convenient to first set the desired amplitude and then set the desired pulse width. Rotation of the PW pot causes the position of the falling edge of the pulse to change.

7) Some properties of the output pulse may change as a function of the amplitude pot setting. For some demanding applications, it may be desirable to use a combination of external attenuators and the amplitude pot to achieve the desired output amplitude.

8) An external clock may be used to control the output PRF of the AVP unit by setting the front panel TRIG toggle switch in the EXT position and applying a 0.2 usec (approx) TTL level pulse to the TRIG TTL BNC connector input. For operation in this mode, the scope time base must also be triggered by the external clock rather than from the SYNC output. The AVP unit may also be triggered externally by applying an ECL level pulse to the TRIG ECL BNC connector.

9) The OUT ECL SMA provides an ECL level pulse to a 50 ohm load terminated in -2.0 volts. The output pulse width is equal to the pulse width provided at the main OUT SMA.

10) To voltage control the output pulse width, remove the jumper wire between banana plugs A and B on the back panel and apply 0 to +10V to connector B ($R_{IN} \geqslant 10K$). (option).

11) To voltage control the output amplitude, remove the jumper wire between banana plugs A and B on the back panel and apply 0 to +10V to connector B ($R_{IN} \geqslant 10K$). (option).

12) For units with the OT or EO options, the output DC offset is variable from +5 to -5 volts by means of the front panel ten turn OFFSET control. The offset control may be turned off by means of the rear panel ON-OFF OFFSET switch.

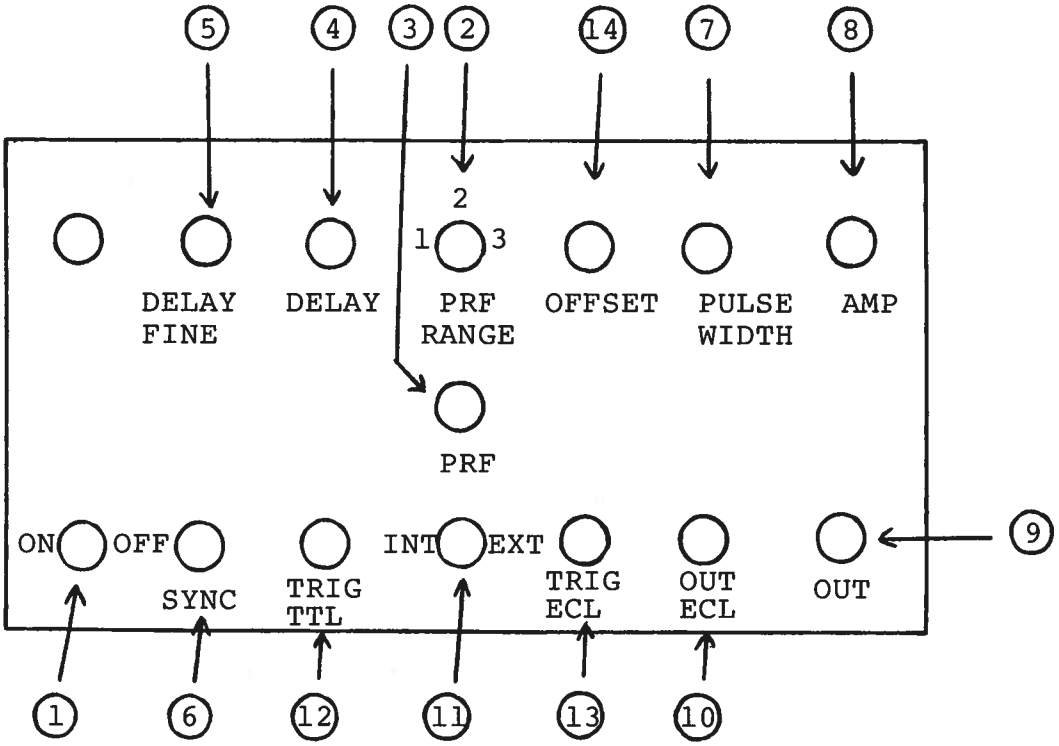
13) For units with the EO option, the output offset may be voltage controlled by removing the jumper wire between banana plugs A and B on the back panel and applying 0 to +10 volts to connector B ($R_{IN} \geqslant 10K$).

14) Dual Polarity Option (for units with the OT or EO options).

To invert the output of the AVP unit, connect the AVX-3-T unit to the OUT port. An inverted pulse is then obtained at the OUT port of the AVX-3-T unit. To offset the inverted pulse, connect a lead from the rear panel OS OUT banana plug to the DC terminal of the AVX-3-T unit. The DC offset at the output of the AVX-3-T unit is then controlled by the front panel OFFSET control.

15) The AVP-C unit can be converted from 110 to 220V 50-60 Hz operation by adjusting the voltage selector card in the rear panel fused voltage selector-cable connector assembly.

Fig. 2 FRONT PANEL CONTROLS



(1) ON-OFF Switch. Applies basic prime power to all stages.

(2) PRF Control. The PRF RANGE and PRF controls determine
(3) output PRF as follows:

	PRF MIN	PRF MAX
Range 1	50 Hz	500 Hz
Range 2	500 Hz	5 KHz
Range 3	5 KHz	50 KHz

(4) DELAY Controls. Controls the relative delay between the
(5) reference output pulse provided at the SYNC output (6) and the main output (9). This delay is variable over the range of 0 to at least 500 nsec.

(6) SYNC Output. This output precedes the main output (9) and is used to trigger the sampling scope time base. The output is a TTL level 100 nsec (approx) pulse capable of driving a fifty ohm load.

(7) PW Control. A ten turn control which varies the output pulse width.

(8) AMP Control. A ten turn control which varies the output pulse amplitude.

(9) OUT. Provides output pulse to fifty ohm load.

(10) OUT ECL. SMA connector provides ECL level output to 50 ohms terminated in -2.0 volts. Pulse width equal to pulse width at OUT (9).

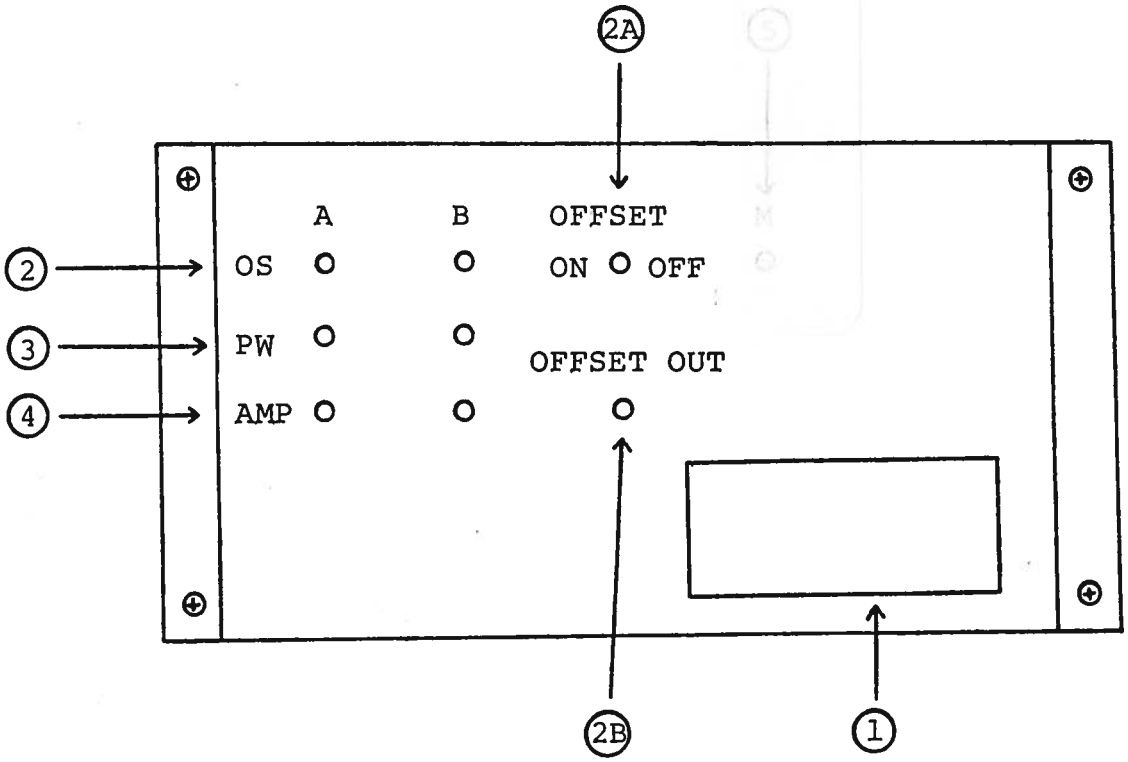
(11) EXT-INT Control. With this toggle switch in the INT position, the PRF of the AVP unit is controlled via an internal clock which in turn is controlled by the PRF controls. With the toggle switch in the EXT position, the AVP unit requires a pulse applied at the TRIG input in order to trigger the output stages. In addition, in this mode, the scope time base must be triggered by the external trigger source.

(12) TRIG TTL Input. A TTL level 0.2 usec external trigger signal is applied at this input when the EXT-INT toggle switch is in the EXT position.

(13) TRIG ECL INPUT. An ECL level trigger signal is applied at this input when the EXT-INT switch is in the EXT position.

(14) OFFSET. A ten turn control for varying the output DC offset from -5 to +5 volts.

Fig. 3 BACK PANEL CONTROLS



(1) FUSED CONNECTOR, VOLTAGE SELECTOR. The detachable power cord is connected at this point. In addition, the removable cord is adjusted to select the desired input operating voltage. The unit also contains the main power fuse.

(2) To voltage control the output DC offset, remove the jumper wire between banana plugs A and B and apply 0 to +10V to connector B ($R_{IN} \geqslant 10K$). (EO option).

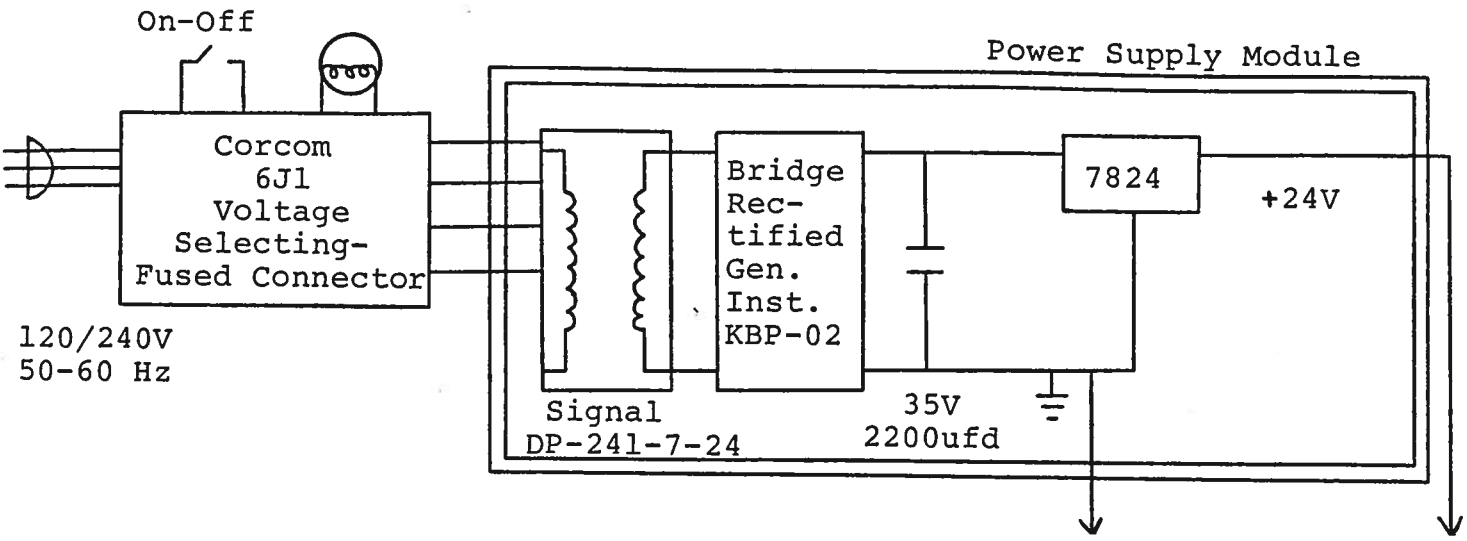
(2A) Two position switch which turns output DC offset ON or OFF. (EO or OT options).

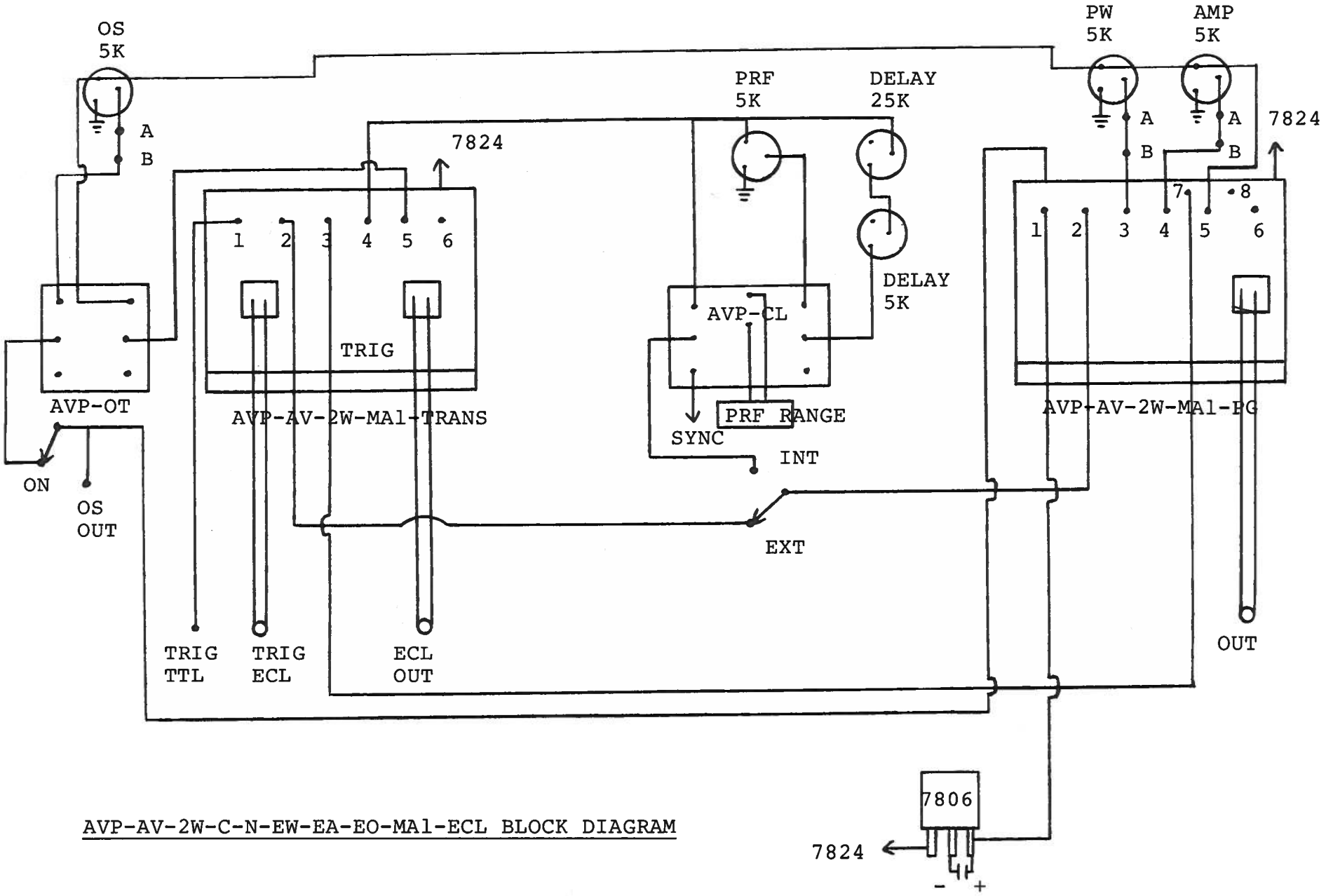
(2B) With OFFSET ON-OFF switch in ON position, DC output offset potential appears at this terminal. To offset inverted pulse on AVP units with dual polarity option (-PN) connect this terminal to the DC terminal of the AVX-3-T module. (EO or OT options).

(3) To voltage control the output pulse width, remove the jumper wire between banana plugs A and B and apply 0 to +10V to connector B ($R_{IN} \geqslant 10K$). (EW option).

(4) To voltage control the output amplitude, remove the jumper wire between banana plugs A and B and apply 0 to +10V to connector B ($R_{IN} \geqslant 10K$). (EA option).

DC POWER SUPPLY





AVP-AV-2W-C-N-EW-EA-EO-MA1-ECL BLOCK DIAGRAM

SYSTEM DESCRIPTION AND REPAIR PROCEDURE (-W UNITS)

The AVP-AV-2-C consists of a pulse generator module (AVP-AV-2-PG), a level translator module (AVP-AV-2-TRAN), an offset module (AVP-OT), a clock module (AVP-AV-2-CL) and a power supply board which supplies +24 volts (600 mA max) to the pulse generator module. In the event that the unit malfunctions, remove the instrument cover by removing the four Phillips screws on the back panel of the unit. The top cover may then be slid off. Measure the voltage at the +24V pin of the PG module. If this voltage is substantially less than +24 volts, unsolder the line connecting the power supply and PG modules and connect 50 ohm 10 W load to the PS output. The voltage across this load should be about +24 V DC. If this voltage is substantially less than 24 volts the PS module is defective and should be repaired or replaced. If the voltage across the resistor is near 24 volts, then the PG module should probably be replaced or repaired. The sealed PG module must be returned to Avtech for repair (or replacement). The clock module provides a 0.1 usec TTL level trigger pulse at pin 2 to trigger the PG module and a 0.1 usec TTL level sync pulse at pin 3 to trigger the sampling scope display device. The output at pin 3 precedes the output at pin 2 by almost 0 to 100 nsec depending on the DELAY control setting. The clock module is powered by +5.8 V supplied by the PG module (from pin 5 to pin 1). With the INT-EXT switch in the EXT position, the clock module is disconnected from the PG module. The clock module is functioning properly if:

a) 0.1 usec TTL level outputs are observed at pins 2 and 3.

b) The PRF of the outputs can be varied over the range of 0.05 KHz to 50 KHz using the PRF and PRF RANGE controls.

c) The relative delay between the pin 2 and 3 outputs can be varied by at least 500 nsec by the DELAY controls.

The sealed clock module must be returned to Avtech for repair or replacement if the above conditions are not observed.

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