AVTECH ELECTROSYSTEMS LTD.

NANOSECOND WAVEFORM ELECTRONICS ENGINEERING · MANUFACTURING

P.O. BOX 265 OGDENSBURG NEW YORK 13669 (315) 472-5270 BOX 5120 STN. "F" OTTAWA, ONTARIO CANADA K2C 3H4 (613) 226-5772 TELEX 053-4591

INSTRUCTIONS

MODEL AVR-A-1-PS-PN PULSE GENERATOR

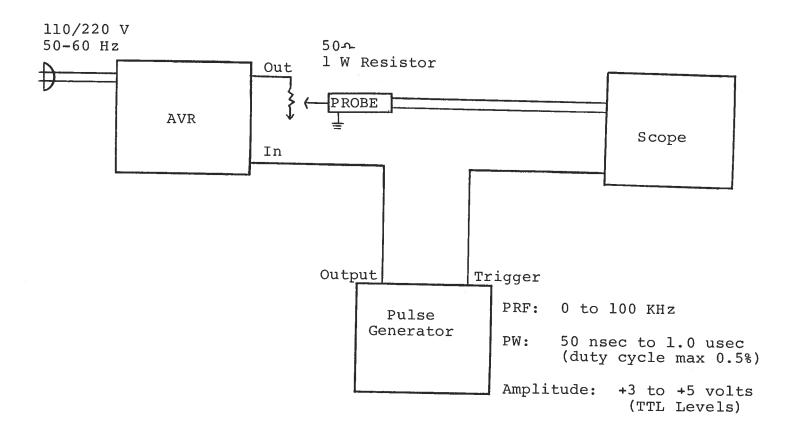
S.N.:

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications OF ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

MODEL AVR-A-1-PS-PN PULSE GENERATOR

TEST ARRANGEMENT



Notes:

- 1) The equipment should be connected in the general fashion shown above. Since the AVR unit provides an output pulse rise time as low as 10 nsec a fast oscilloscope (at least 50 MHz and preferably 200 MHz) should be used to display the waveform. Also, if a load of other than 50 ohm is employed, the length of coaxial cable between the AVR unit and the load should not exceed about 5 feet or the output waveform may be degraded by the resulting reflections.
- 2) The output PRF is equal to the input trigger pulse PRF.
- 3) When triggering the AVR from a high speed lab pulse generator it may be necessary to shunt the input to the AVR by a 50 ohm resistor to eliminate reflection which may interfere with the operation of the lab pulse generator.
- 4) In general, the source pulse generator trigger delay control should be set in the 0.1 to 1.0 usec range. Other settings should be as shown in the above diagram.
- 5) WARNING: Model AVR may fail if triggered at a PRF greater than 100 KHz or if the duty cycle exceeds 0.5% or if the PW exceeds 1.0 usec.
- The output amplitude is controlled by means of the one turn potentiometer (AMP).
- 7) The output pulse width is approximately equal to the input pulse width.
- 8) The desired output polarity is selected by means of the POLARITY switch. With the POLARITY switch in the P position, the negative output pulse generator is rendered inactive. Likewise, with the POLARITY switch in the N position, the positive pulse generator is rendered inactive.

SYSTEM DESCRIPTION AND REPAIR PROCEDURE

The AVR consists of two pulse generator modules (POS and NEG) and a power supply board which supplies +24 volts (600 mA max) to the pulse generator module. In the event that the unit malfunctions, remove the instrument cover by removing the four Phillips screws on the back side of the unit. The top lid may then be slid off. Measure the voltage at the +24V pin of the PG module. If this voltage is substantially less than +24 volts, unsolder the line connecting the power supply and PG modules and connect 50 ohm 10 W load to the PS output. The voltage across this load should be about +24V DC. If this voltage is substantially less than 24 volts the PS module is defective and should be repaired or replaced. If the voltage across the resistor is near 24 volts, then the SL4 switching elements in the AVR-PG module have probably failed. The SL4 switching elements are easily replaced by removing the cover plate on the instrument bottom side and extracting the SL4 switching elements from their sockets using a pair of needle nose pliers. Before attempting this first insure that the prime power is off and also briefly ground the metal tabs on the SL4 elements to the chassis as bypass capacitors may be charged to 225 volts. the Replacement SL4 units must be ordered directly from Avtech. When reinstalling the SL4 units in their sockets, insure that the shortest of the three terminals is adjacent to the black dot on the AVR-PG chassis.

SYSTEM BLOCK DIAGRAM

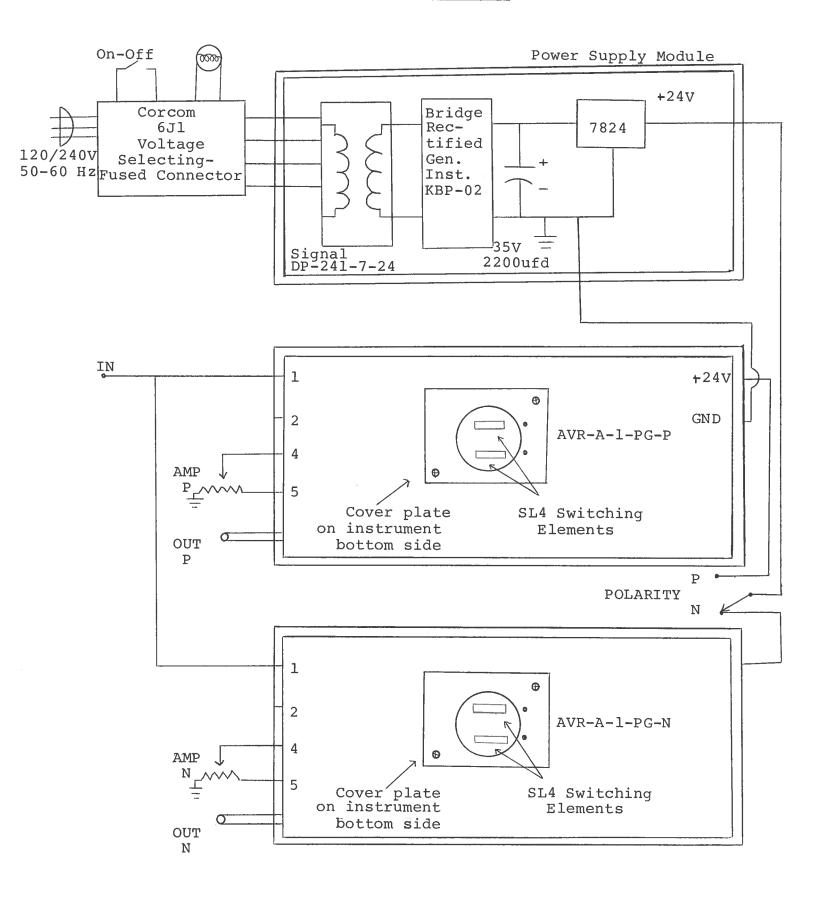


Fig. 2

