

AVTECH ELECTROSYSTEMS LTD.

NANOSECOND WAVEFORM ELECTRONICS
ENGINEERING - MANUFACTURING

□ P.O. BOX 265
OGDENSBURG
NEW YORK
13669
(315) 472-5270

☒ BOX 5120, STN. "F"
OTTAWA, ONTARIO
CANADA K2C 3H4
TEL: (613) 226-5772
FAX: (613) 226-2802
TELEX: 053-4591

INSTRUCTIONS

MODEL AVR-B4-C PULSE GENERATOR

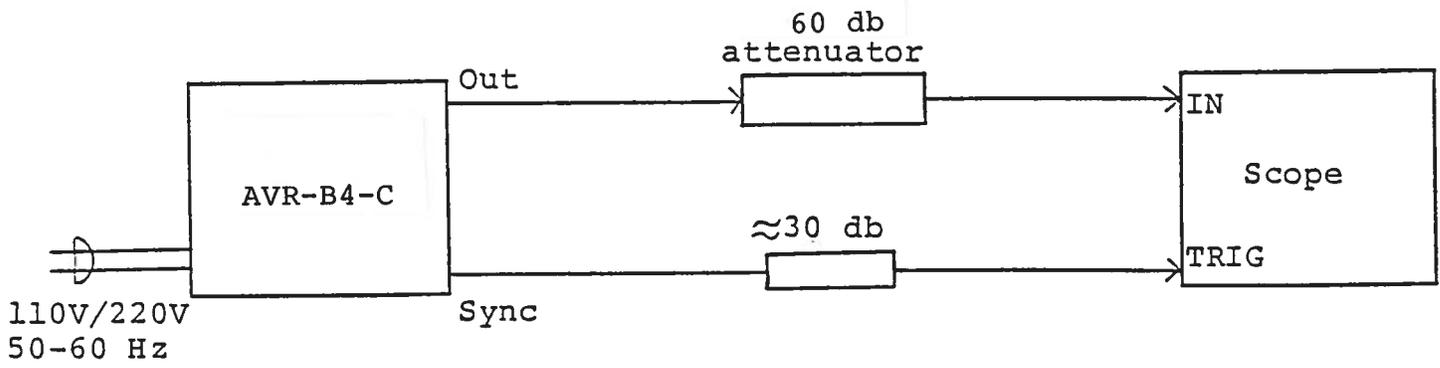
S.N. :

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been disassembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

Fig. 1

PULSE GENERATOR TEST ARRANGEMENT

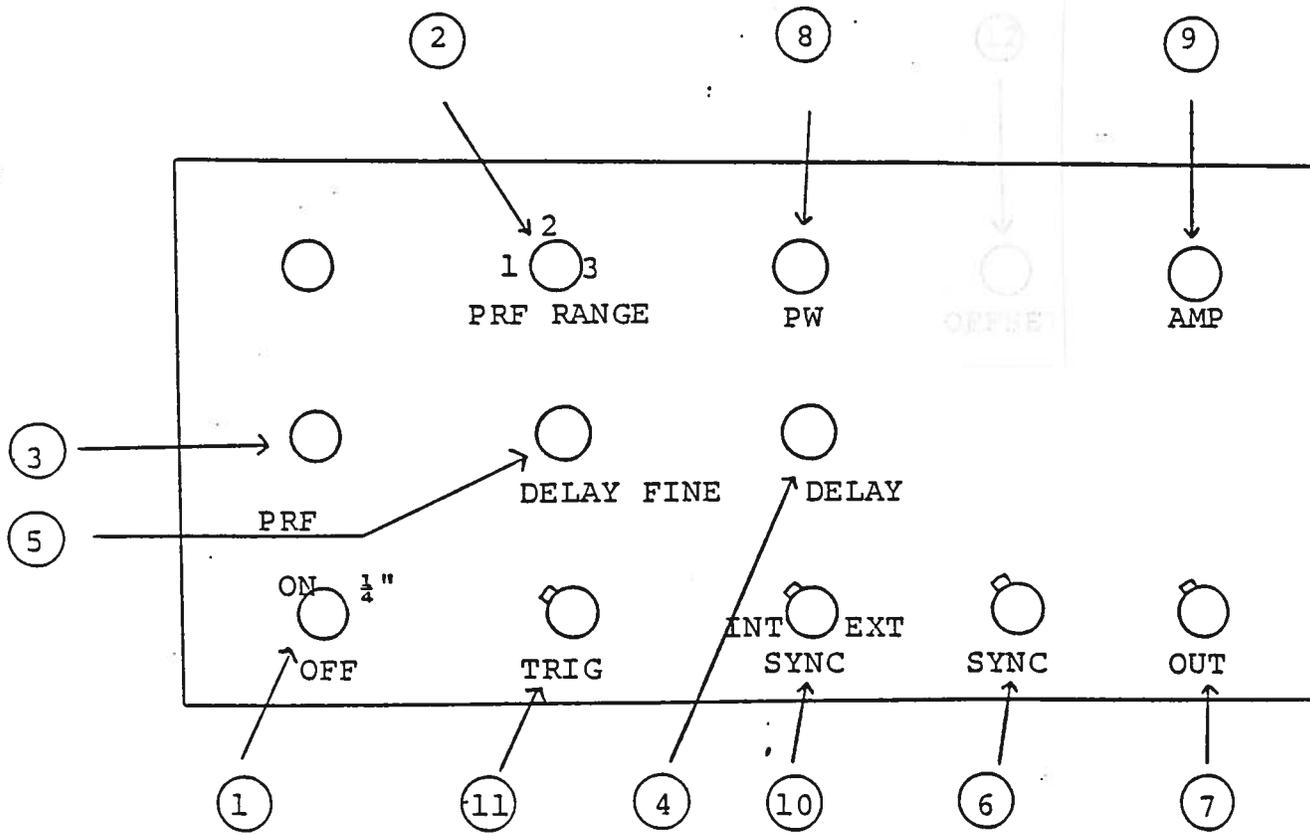


Notes:

- 1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed 200 MHz.
- 2) The use of 60 db attenuator at the scope vertical input channel will insure a peak input signal to the scope of less than one volt (necessary only if sampling scope used). If a high impedance real time scope is used, the pulse generator should be terminated using a shunt 50 ohm resistor.
- 3) The sync output channel provides TTL level signals. To avoid overdriving the TRIG input channel of some scopes, a 30 db attenuator should be placed at the input to the scope trigger channel.
- 4) To obtain a stable output display the PW and PRF controls on the front panel should be set maximum counter-clockwise while the front panel PRF RANGE switch may be in either range. The front panel TRIG toggle switch should be in the INT position. The DELAY controls and the scope triggering controls are then adjusted to obtain a stable output. The scope may then be used to set the desired PRF by rotating the PRF control and by means of the PRF RANGE switch.
- 5) The output pulse width is controlled by means of the front panel one turn PW control. The control should initially be set maximum counter-clockwise and the pulse width adjusted using an oscilloscope.
- 6) The output pulse amplitude is controlled by means of the front panel one turn AMP control.
- 7) To voltage control the output pulse width, set the rear panel switch in the EXT position and apply 0 to +10V between A terminal and ground ($R_{IN} \geq 10K$). (option).
- 8) To voltage control the output amplitude, set the rear panel switch in the EXT position and apply 0 to +10V between A terminal and ground ($R_{IN} \geq 10K$). (option).
- 9) To DC offset the output pulse connect a DC power supply set to required DC offset value to the back panel terminals marked O.S. The maximum attainable DC offset voltage is ± 50 volts (100 mA max).
- 10) An external clock may be used to control the output PRF of the AVR unit by setting the front panel TRIG toggle switch in the EXT position and applying a 0.2 usec (approx.) TTL level pulse to the TRIG BNC connector input. For operation in this mode, the scope time base must also be triggered by the external clock rather than from the SYNC output.

Fig. 2

FRONT PANEL CONTROLS

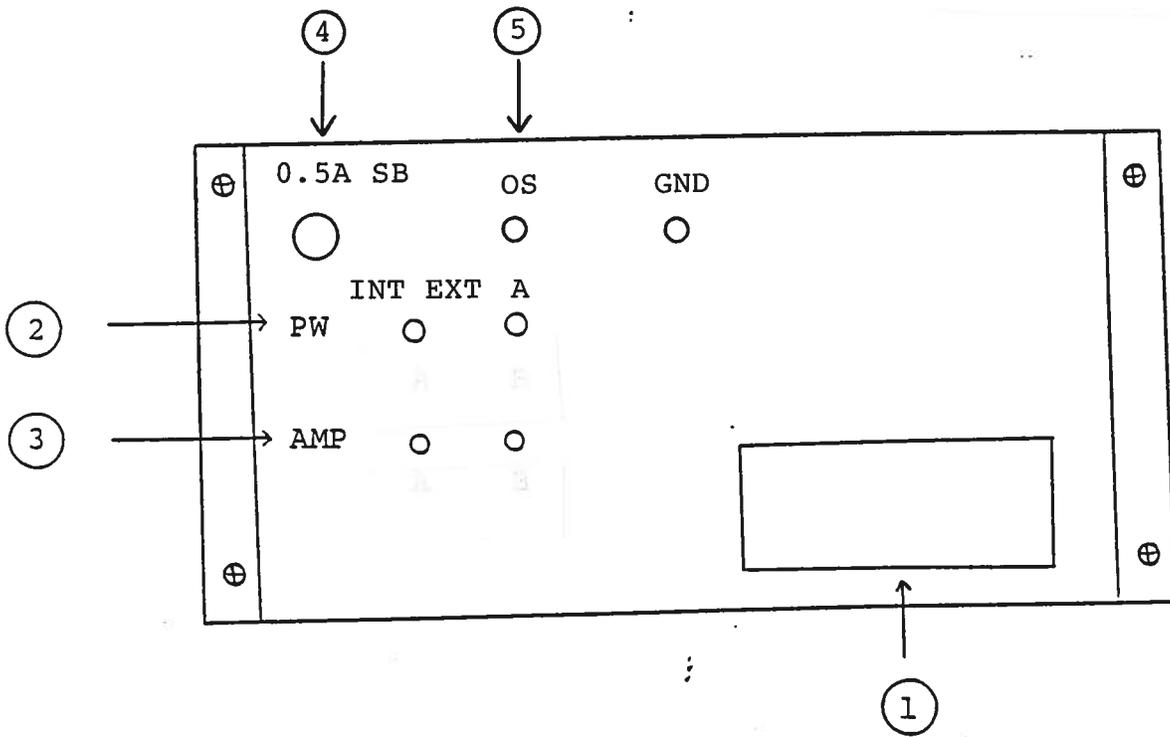


- (1) ON-OFF Switch. Applies basic prime power to all stages.
- (2) PRF Control. With the PRF range switch in 1 position,
- (3) PRF control will vary PRF from 0.10 KHz to about 1.0 KHz. With the PRF RANGE switch in 2 position, varies PRF from about 1.0 KHz to about 10 KHz. With the PRF RANGE switch in the 3 position, varies PRF from about 10 KHz to 100 KHz. The operating PRF should be set using a scope.
- (4) DELAY Control. Controls the relative delay between the reference output pulse provided at the SYNC output (6) the main output (7). This delay is variable over the range of 0 to at least 500 nsec.
- (5) DELAY FINE. As DELAY (4) but about 5 times less sensitive.
- (6) SYNC Output. This output precedes the main output (7) and is used to trigger the scope time base. The output is a TTL level 100 nsec (approx.) pulse capable of driving a fifty ohm load. The relative delay between the SYNC output and the main output is variable from 0 to 500 nsec using the DELAY controls.
- (7) OUT Connector. BNC connector provides output to a fifty ohm load.
- (8) PW Control. A one turn control which varies the output pulse width.
- (9) AMP Control. A one turn control which varies the output pulse amplitude.
- (10) EXT-INT Control. With this toggle switch in the INT position, the PRF of the AVR unit is controlled via an internal clock which in turn is controlled by the PRF and PRF FINE controls. With the toggle switch in the EXT position, the AVR unit requires a 0.2 usec TTL level pulse applied at the TRIG input in order to trigger the output stages. In addition, in this mode, the scope time base must be triggered by the external trigger source.
- (11) TRIG Input. The external trigger signal is applied at this input when the EXT-INT toggle switch is in the EXT position.

Fig. 3

BACK PANEL CONTROLS

(FOR UNITS WITHOUT THE
OT OR ED OPTIONS)

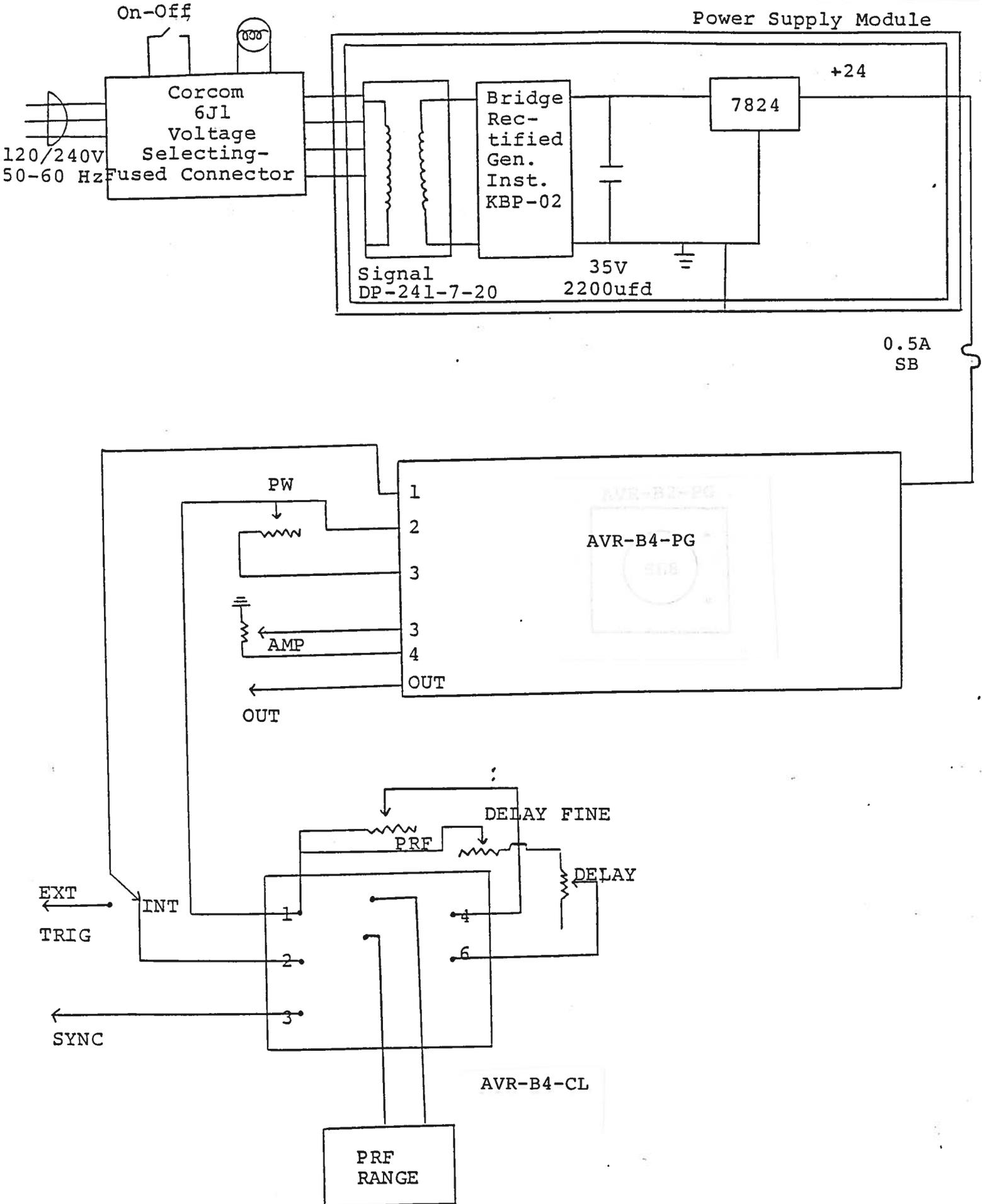


- (1) FUSED CONNECTOR, VOLTAGE SELECTOR. The detachable power cord is connected at this point. In addition, the removable cord is adjusted to select the desired input operating voltage. The unit also contains the main power fuse.
- (2) To voltage control the output pulse width, set the rear panel switch in the EXT position and apply 0 to +10V between A terminal and ground ($R_{IN} \gg 10K$). (option).
- (3) To voltage control the output amplitude, set the rear panel switch in the EXT position and apply 0 to +10V between A terminal and ground ($R_{IN} \gg 10K$). (option).
- (4) 0.5A SB. This fuse limits the DC prime power supplied to the output stage and will blow in the case of severe overloading.
- (5) OS. To DC offset the output pulse connect a DC power supply set to required DC offset value to the OS terminals. The maximum attainable DC offset voltage is ± 50 volts (100 mA max).

Fig. 4

SYSTEM BLOCK DIAGRAM

(FOR UNITS WITHOUT THE SA & SO OPTIONS)



SYSTEM DESCRIPTION AND REPAIR PROCEDURE

The AVR-B4-C consists of the following basic modules:

- 1) AVR-B4-PG pulse generator module
- 2) AVR-B4-CL clock module
- 3) +24V power supply board

The modules are interconnected as shown in Fig. 4. The clock module controls the output PRF and the relative delay between the main output and the SYNC outputs. The PW pulse generator modules generate the output pulse. In the event of an instrument malfunction, it is most likely that the rear panel 0.5A SB fuse may have failed due to an output short circuit condition or to a high duty cycle condition.

- a) 0.1 usec TTL level outputs are observed at pins 2 and 3.
- b) The PRF of the outputs can be varied over the range of 0.1 KHz to 100 KHz using the PRF & PRF FINE and PRF RANGE controls.
- c) The relative delay between the pin 2 and 3 outputs can be varied by at least 500 nsec by the DELAY controls.

The sealed clock module must be returned to Avtech for repair or replacement if the above conditions are not observed. The power supply board generates +24V DC to power the other modules. If the voltage is less than +24V, turn off the prime power and unsolder the lead from the 7824 regulator chip on the power supply board. Solder a 100 ohm 5 watt resistor to the 7824 output to ground and turn on the prime power. A voltage of +24 volts should be read. If the voltage is less then the power supply board is defective and should be repaired or replaced.

Schroff

08.28.89

-EW

-EA

-OS

1. The test equipment used is described in the following table:

2. The test results are given in the following table:

3. The test results are given in the following table:

The test results are given in the following table:

The test results are given in the following table:

The test results are given in the following table: