AVTECH ELECTROSYSTEMS LTD.

NANOSECOND WAVEFORM ELECTRONICS
ENGINEERING – MANUFACTURING

P.O. BOX 265
OGDENSBURG
NEW YORK
13669
(315) 472-5270

BOX 5120, STN. "F"
OTTAWA, ONTARIO
CANADA K2C 3H4
TEL: (613) 226-5772
FAX: (613) 226-2802
TELEX: 053-4591

INSTRUCTIONS

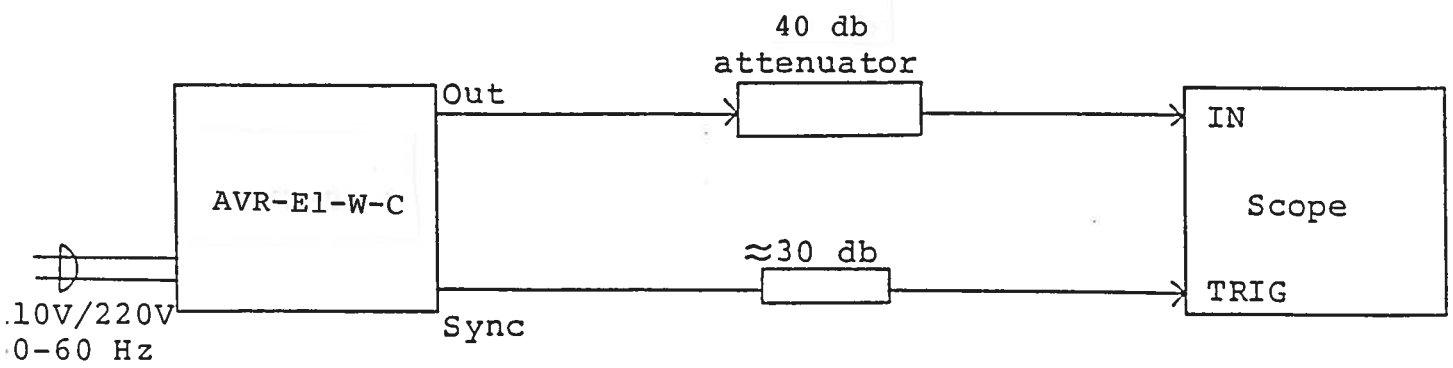
MODEL AVR-E1-W-C-OT PULSE GENERATOR

S.N.:

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

Fig. 1 PULSE GENERATOR TEST ARRANGEMENT



Notes:

1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed 2 GHz.

2) The use of 40 db attenuator at the scope vertical input channel will insure a peak input signal to the scope of less than one volt (necessary only if sampling scope used). If a high impedance real time scope is used, the pulse generator should be terminated using a shunt 50 ohm resistor.

3) The sync output channel provides TTL level signals. To avoid overdriving the TRIG input channel of some scopes, a 30 db attenuator should be placed at the input to the scope trigger channel. The SYNC output precedes the main output when the front panel LEAD-LAG switch is in the LEAD position. The SYNC output lags the main output when the switch is in the LAG position.

4) To obtain a stable output display the PW and PRF controls on the front panel should be set mid range. The front panel TRIG toggle switch should be in the INT position. The DELAY controls and the scope triggering controls are then adjusted to obtain a stable output. The scope may then be used to set the desired PRF by rotating the PRF controls.

5) The output pulse width is controlled by means of the front panel one turn PW control. To voltage control the pulse width, set the rear panel switch in the EXT position and apply 0 to +10 volts between terminal A and ground (R_{IN} > 10K). (option).

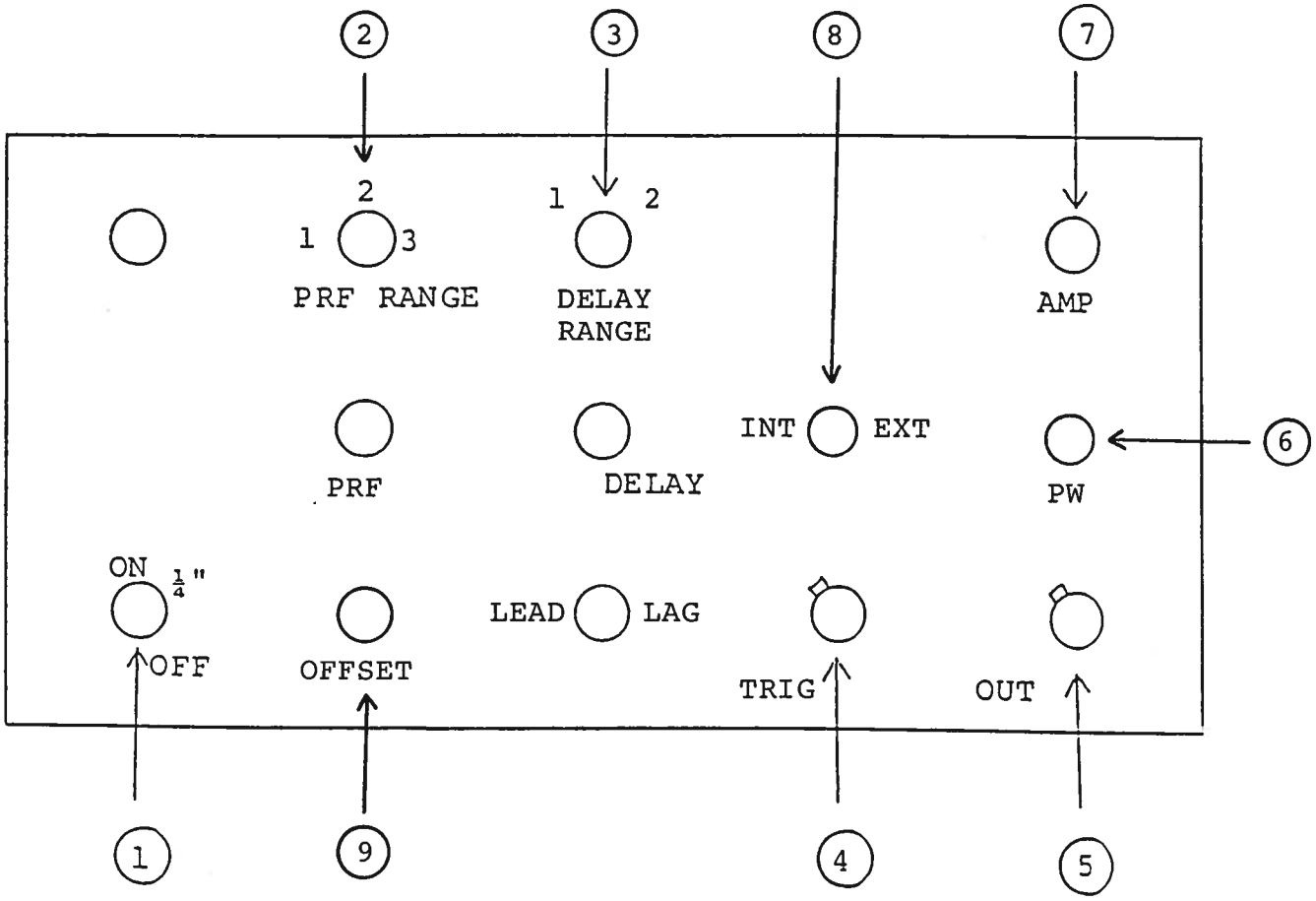
6) The output pulse amplitude is controlled by means of the front panel one turn AMP control. To voltage control the output, set the rear panel switch in the EXT position and apply 0 to +10 volts between terminal A and ground (R_{IN} > 10K). (option).

7) An external clock may be used to control the output PRF of the AVR unit by setting the front panel TRIG toggle switch in the EXT position and applying a 0.2 usec (approx.) TTL level pulse to the TRIG BNC connector input. For operation in this mode, the scope time base must also be triggered by the external clock rather than from the SYNC output.

8) For units with the OT offset option, the output DC offset level is varied from -5 to +5V (to 50 ohm) by the front panel OFFSET one turn control. The DC offset may be turned off using the rear panel OS ON-OFF toggle switch. (OT option).

Fig. 2

FRONT PANEL CONTROLS



(1) ON-OFF Switch. Applies basic prime power to all stages.

(2) PRF Control. Varies PRF as follows:

	MIN	MAX
Range 1	20 Hz	200 Hz
Range 2	200 Hz	2 KHz
Range 3	2 KHz	20 KHz

The operating PRF should be set using a scope.

(3) DELAY Control. Controls the relative delay between the reference output pulse provided at the TRIG output (4) the main output (5). This delay is variable over the range of 0 to about 1.0 usec (RANGE 1) and 1.0 to 5.0 usec (RANGE 2). The TRIG output precedes the main output when the LEAD-LAG switch is in the LEAD position and lags when the switch is in the LAG position.

(4) TRIG Output. This output is used to trigger the scope time base. The output is a TTL level 100 nsec (approx.) pulse capable of driving a fifty ohm load.

(5) OUT Connector. SMA connector provides output to a fifty ohm load.

(6) PW Control. A one turn control which varies the output pulse width from 100 nsec to 5 usec.

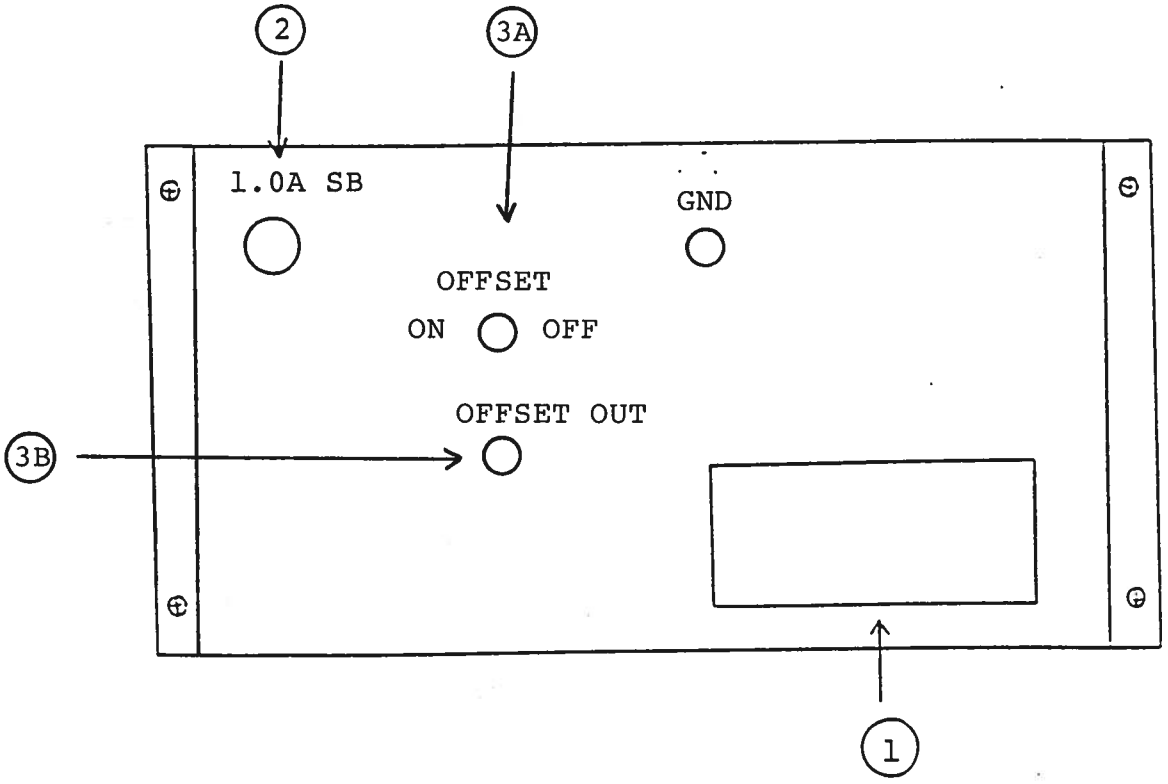
(7) AMP Control. A one turn control which varies the output pulse amplitude from 0 to 20V to a fifty ohm load.

(8) EXT-INT Control. With this toggle switch in the INT position, the PRF of the AVR unit is controlled via an internal clock which in turn is controlled by the PRF controls. With the toggle switch in the EXT position, the AVR unit requires a 0.2 usec TTL level pulse applied at the TRIG input in order to trigger the output stages. In addition, in this mode, the scope time base must be triggered by the external trigger source.

(9) OFFSET. For units with the OT or EO offset option, the output DC offset level is varied from -5 to +5V (to 50 ohm) by the front panel OFFSET one turn control. The DC offset may be turned off using the rear panel OS ON-OFF toggle switch.

Fig. 3

BACK PANEL CONTROLS



(1) FUSED CONNECTOR, VOLTAGE SELECTOR. The detachable power cord is connected at this point. In addition, the removable cord is adjusted to select the desired input operating voltage. The unit also contains the main power fuse (0.5A SB).

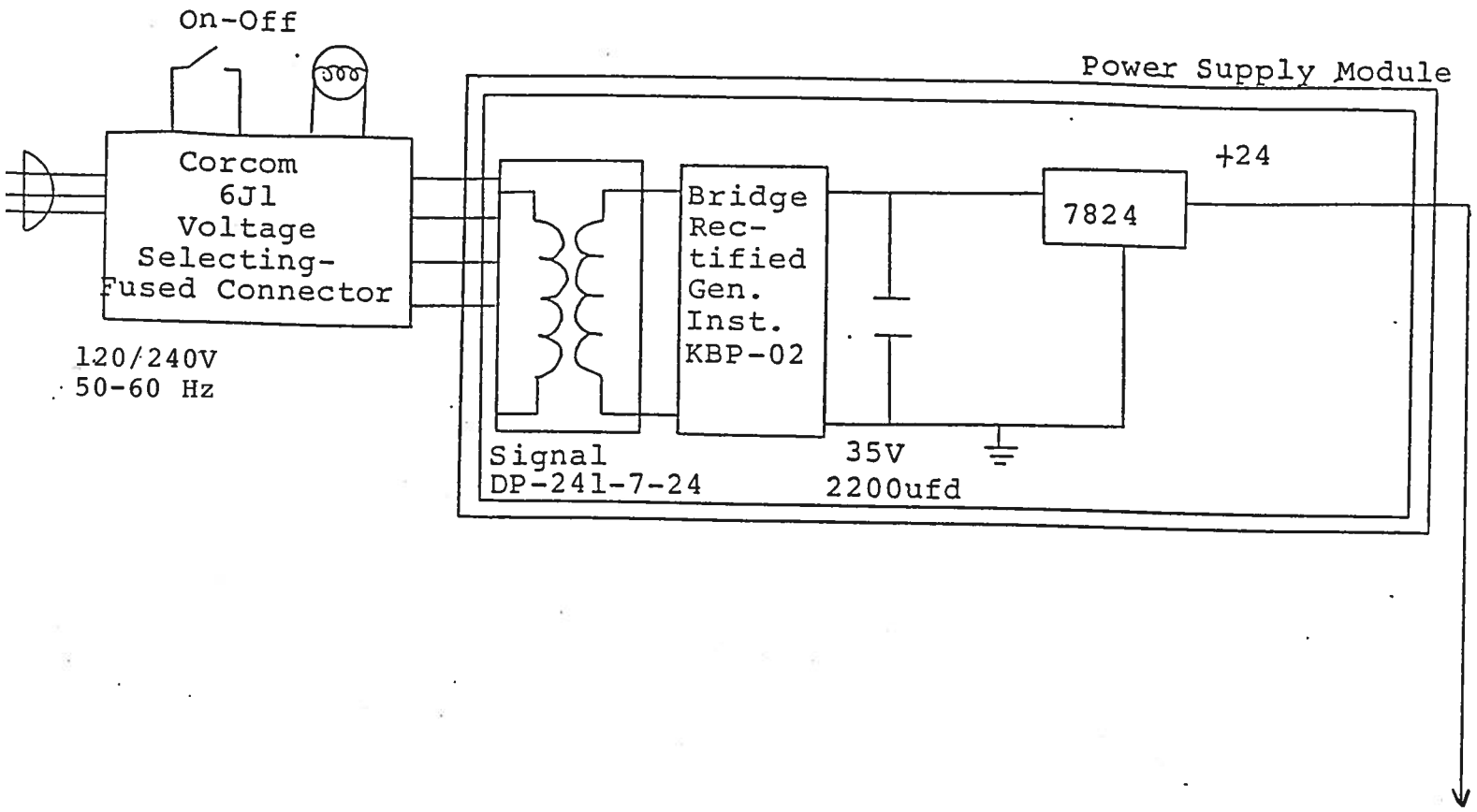
(2) 1.0A SB. Fuse which protects the output stage if the output duty cycle rating is exceeded.

(3A) Two position switch which turns output DC offset ON or OFF. (EO or OT options).

(3B) With OFFSET ON-OFF switch in ON position, DC output offset potential appears at this terminal.

Fig. 4

SYSTEM BLOCK DIAGRAM



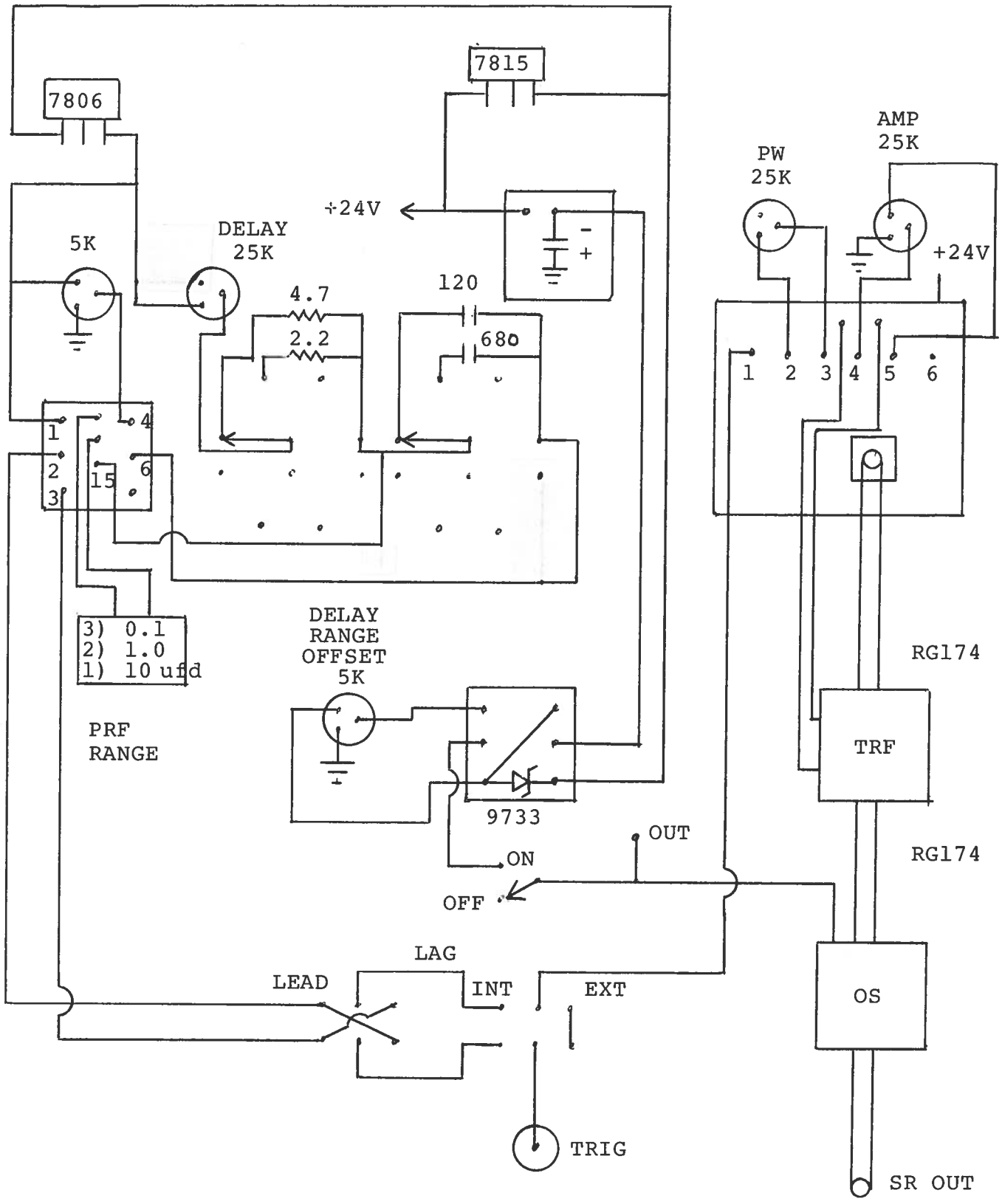


Fig. 5 AVR-E1-W-C-P-OT (GGB MOD)

SYSTEM DESCRIPTION AND REPAIR PROCEDURE

The AVR-E1-W-C consists of the following basic modules:

1) AVR-E1-W-PG pulse generator module
2) AVR-E1-CL clock module
3) +24V power supply board
4) AVR-E1-PS-15 power supply module
5) AVR-E1-OT offset module
6) AVR-E1-GGB-TRF offset module
7) AVR-E1-W-OS offset module

The modules are interconnected as shown in Fig. 5.

In the event that the unit malfunctions, remove the instrument cover by removing the four Phillips screws on the back panel of the unit. The top cover may then be slid off. Measure the voltage at the +24 V pin of the PG module. If this voltage is substantially less than +24 volts, unsolder the line connecting the power supply and PG modules and connect 100 ohm 10 W load to the PS output. The voltage across this load should be about +24 V DC. If this voltage is substantially less than 24 volts the PS module is defective and should be repaired or replaced. If the voltage across the resistor is near 24 volts, then the PG module should be replaced or repaired. The sealed PG module must be returned to Avtech for repair (or replacement). The clock module provides a 0.1 usec TTL level trigger pulse at Pin 2 to trigger the PG module and a 0.1 usec TTL level sync pulse at Pin 3 to trigger the sampling scope display device. The output at Pin 3 precedes the output at Pin 2 by almost 0 to 5 usec depending on the DELAY control setting. The clock module is powered by +5.8 V supplied by the PG module (from Pin 2 to Pin 1). With the INT-EXT switch in the EXT position, the clock module is disconnected from the PG module. The clock module is functioning properly if:

a) 0.1 usec TTL level outputs are observed at Pins 2 and 3.

b) The PRF of the outputs can be varied over the range of 20 Hz to 20 KHz using the PRF and PRF RANGE controls.

c) The relative delay between the Pin 2 and 3 outputs can be varied by at least 5 usec by the DELAY controls.

The sealed clock module must be returned to Avtech for repair or replacement if the above conditions are not observed.

Schroff 03.06.90

- EW
- EA
- EO
- OT