AVTECH ELECTROSYSTEMS LTD.

NANOSECOND WAVEFORM ELECTRONICS
ENGINEERING – MANUFACTURING

P.O. BOX 265
OGDENSBURG
NEW YORK
13669
(315) 472-5270

BOX 5120, STN. "F"
OTTAWA, ONTARIO
CANADA K2C 3H4
TEL: (613) 226-5772
FAX: (613) 226-2802

INSTRUCTIONS

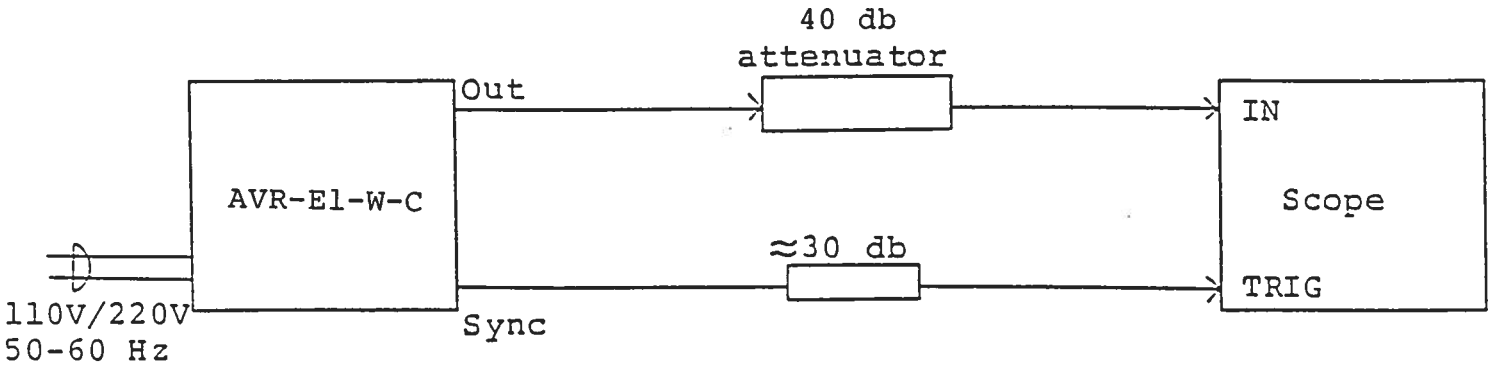
MODEL AVR-E2-C PULSE GENERATOR

S.N.:

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

Fig. 1 PULSE GENERATOR TEST ARRANGEMENT



Notes:

1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed 2 GHz.

2) The use of 50 db attenuator at the scope vertical input channel will insure a peak input signal to the scope of less than one volt (necessary only if sampling scope used). If a high impedance real time scope is used, the pulse generator should be terminated using a shunt 50 ohm resistor.

3) The sync output channel provides TTL level signals. To avoid overdriving the TRIG input channel of some scopes, a 30 db attenuator should be placed at the input to the scope trigger channel. The SYNC output precedes the main output when the front panel LEAD-LAG switch is in the LEAD position. The SYNC output lags the main output when the switch is in the LAG position.

4) To obtain a stable output display the PW and PRF controls on the front panel should be set mid range. The front panel TRIG toggle switch should be in the INT position. The DELAY controls and the scope triggering controls are then adjusted to obtain a stable output. The scope may then be used to set the desired PRF by rotating the PRF controls.

5) The output pulse width is controlled by means of the front panel one turn PW control.

5A) EW option: To voltage control the pulse width, set the rear panel switch in the eXT position and apply 0 to +10 volts between terminal A and ground (R_{IN} > 10K). (option).

5B) EWD option: To digitally control the output pulse width (in 256 increments) set the rear panel switch in the EXT position and apply a parallel TTL control to PINS 1 to 8 (PIN 1 = LSB, PIN 8 = MSB) to the rear panel D connector.

6) The output pulse amplitude is controlled by means of the front panel one turn AMP control.

6A) EA option: To voltage control the output, set the rear panel switch in the EXT position and apply 0 to +10 volts between terminal A and ground (R_{IN} > 10K). (option).

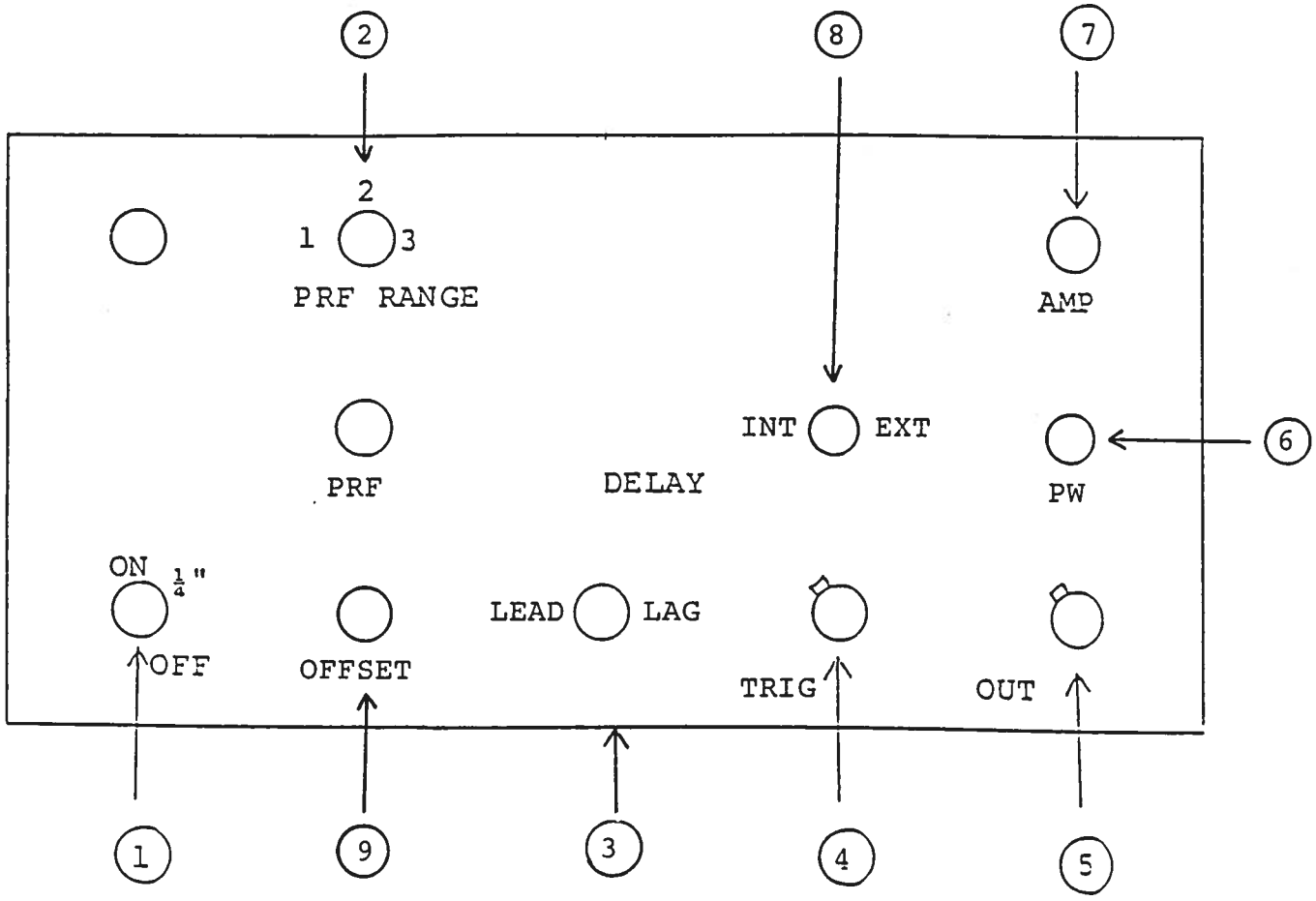
6B) EAD option: To digitally control the output amplitude (in 256 increments) set the rear panel switch in the EXT position and apply a parallel TTL control to PINS 9 to 16 (PIN 9 = LSB, PIN 8 = MSB) to the rear panel D connector.

7) An external clock may be used to control the output PRF of the AVR unit by setting the front panel TRIG toggle switch in the EXT position and applying a 0.2 usec (approx.) TTL level pulse to the TRIG BNC connector input. For operation in this mode, the scope time base must also be triggered by the external clock rather than from the SYNC output.

8) For units with the OT offset option, the output DC offset level is varied from -5 to +5V (to 50 ohm) by the front panel OFFSET one turn control. The DC offset may be turned off using the rear panel OS ON-OFF toggle switch. (OT option).

Fig. 2

FRONT PANEL CONTROLS



(1) ON-OFF Switch. Applies basic prime power to all stages.

(2) PRF Control. Varies PRF as follows:

	MIN	MAX
Range 1	50 Hz	500 Hz
Range 2	500 Hz	5 KHz
Range 3	5 KHz	50 KHz

The operating PRF should be set using a scope.

(3) DELAY Control. Controls the relative delay between the reference output pulse provided at the TRIG output (4) the main output (5). This delay is variable over the range of 0 to about 1.0 usec. The TRIG output precedes the main output when the LEAD-LAG switch is in the LEAD position and lags when the switch is in the LAG position.

(4) TRIG Output. This output is used to trigger the scope time base. The output is a TTL level 100 nsec (approx.) pulse capable of driving a fifty ohm load.

(5) OUT Connector. SMA connector provides output to a fifty ohm load.

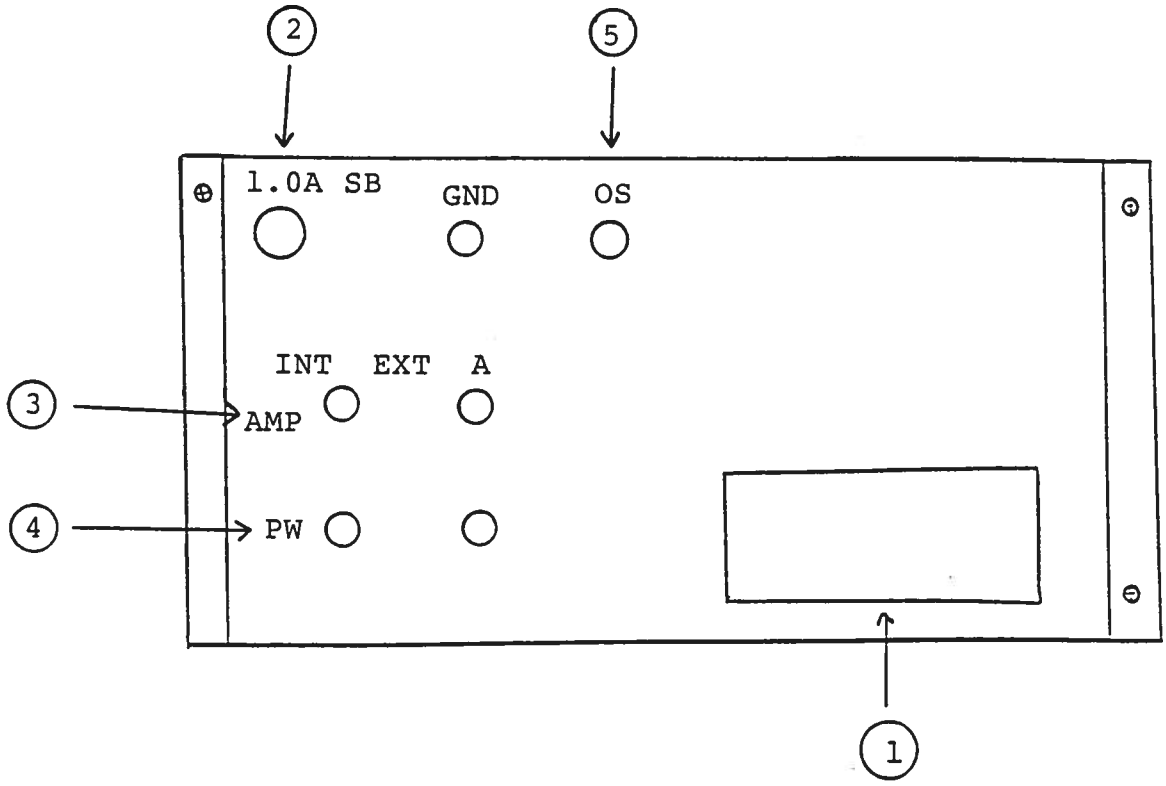
(6) PW Control. A one turn control which varies the output pulse width.

(7) AMP Control. A one turn control which varies the output pulse amplitude to a fifty ohm load.

(8) EXT-INT Control. With this toggle switch in the INT position, the PRF of the AVR unit is controlled via an internal clock which in turn is controlled by the PRF controls. With the toggle switch in the EXT position, the AVR unit requires a 0.2 usec TTL level pulse applied at the TRIG input in order to trigger the output stages. In addition, in this mode, the scope time base must be triggered by the external trigger source.

(9) OFFSET. For units with the OT or EO offset option, the output DC offset level is varied from -5 to +5V (to 50 ohm) by the front panel OFFSET one turn control. The DC offset may be turned off using the rear panel OS ON-OFF toggle switch.

Fig. 3 BACK PANEL CONTROLS (for units without EWD and EAD options)



(1) FUSED CONNECTOR, VOLTAGE SELECTOR. The detachable power cord is connected at this point. In addition, the removable cord is adjusted to select the desired input operating voltage. The unit also contains the main power fuse.

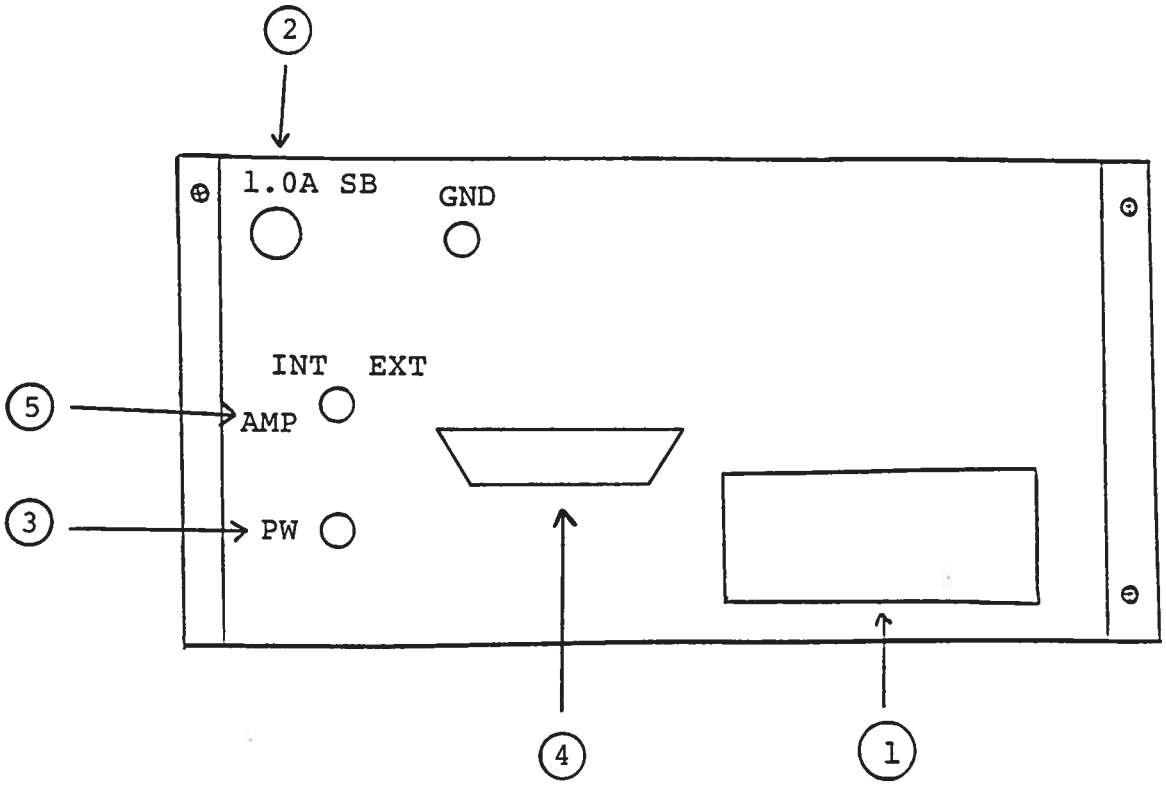
(2) 1.0A SB. Fuse which protects the output stage if the output duty cycle rating is exceeded.

(3) EA. To voltage control the output amplitude, set the switch in the EXT position and apply 0 to +10 volts between terminal A and ground ($R_{IN} \geqslant 10K$). (option).

(4) EW. To voltage control the output pulse width, set the switch in the EXT position and apply 0 to +10 volts between terminal A and ground ($R_{IN} \geqslant 10K$). (option).

(5) DC OFFSET Input. To DC offset the output pulse, connect a DC power supply set to the desired offset value to these terminals. The maximum allowable DC offset voltage is $\pm$50 volts, $\pm$200 mA. (option).

Fig. 3 BACK PANEL CONTROLS (for units with the EWD and EAD options)



(1) FUSED CONNECTOR, VOLTAGE SELECTOR. The detachable power cord is connected at this point. In addition, the removable cord is adjusted to select the desired input operating voltage. The unit also contains the main power fuse.

(2) 1.0A SB. Fuse which protects the output stage if the output duty cycle rating is exceeded.

(3) EWD option: To digitally control the output pulse width (in 256 increments) set the rear panel switch (3) in the EXT position and apply a parallel TTL control to PINS 1 to 8 (PIN 1 = LSB, PIN 8 = MSB) to the D connector (4). PIN 24 is ground.

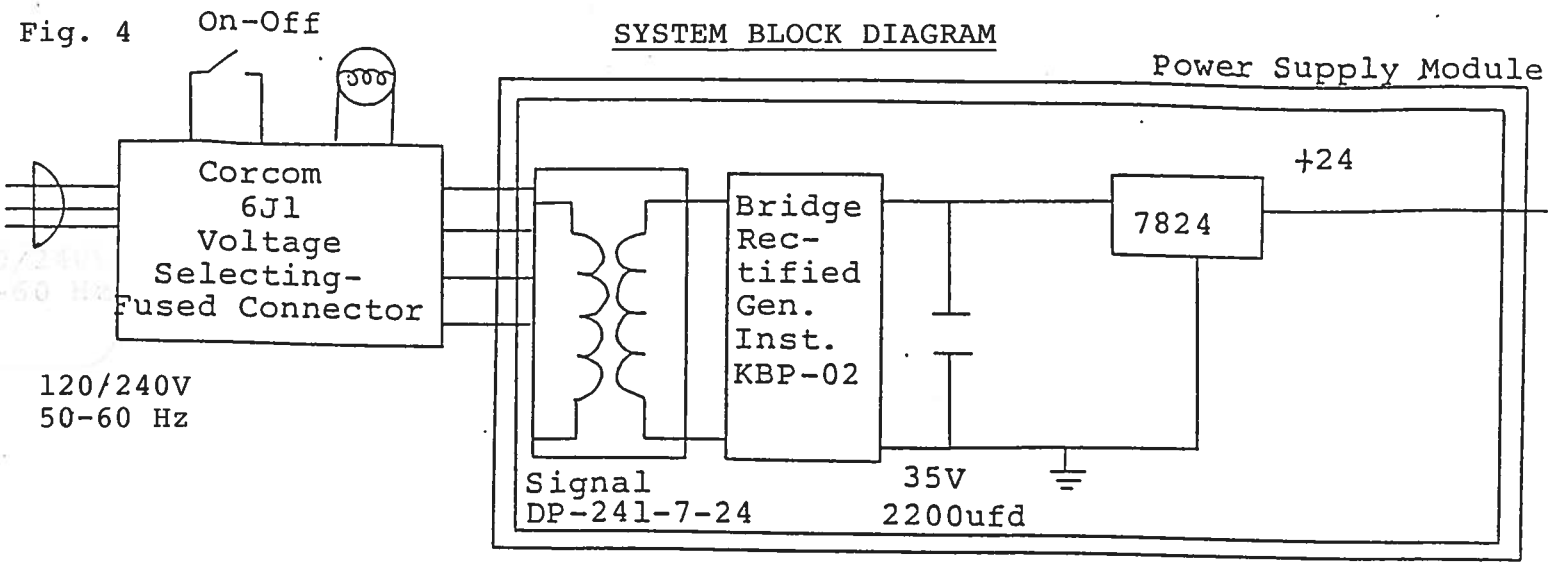
Logic Level	Volts	Current
0	0 to +0.8V	10 uA (max)
1	+2 to +5V	10 uA (max)

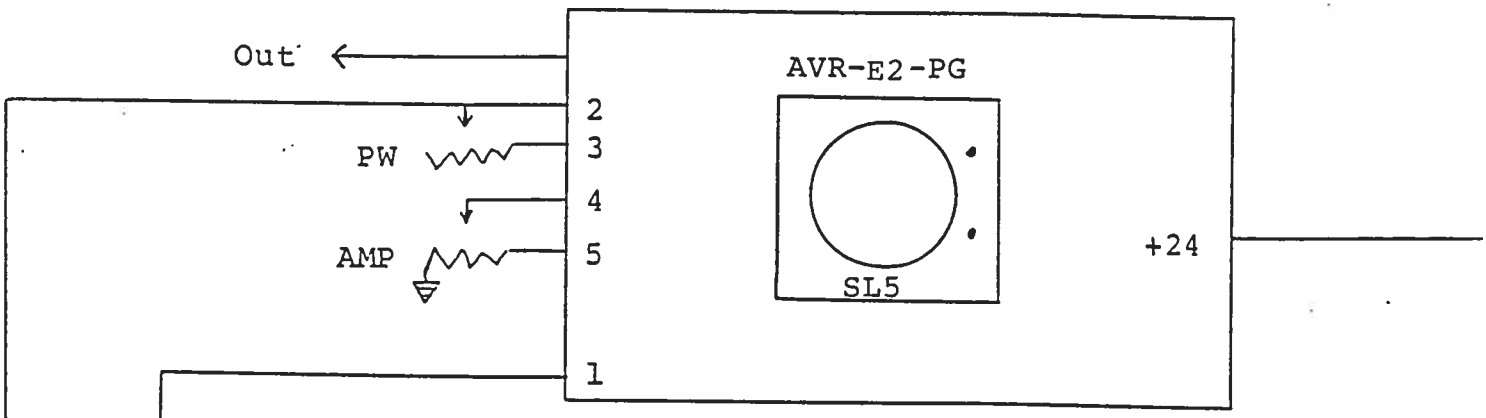
(4) EWD, EAD D Connector. 24 PIN amphenol panel receptacle No. 57-40240. Mates with 57-50240.

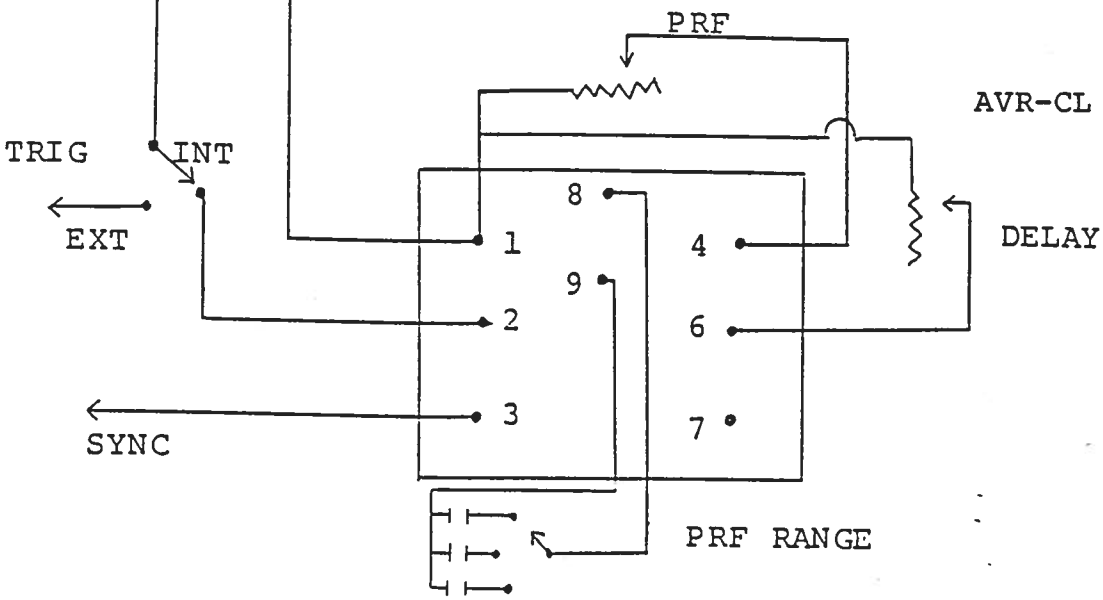
(5) EAD option: To digitally control the output amplitude (in 256 increments) set the switch (5) in the EXT position and apply a parallel TTL control to PINS 9 to 16 (PIN 9 = LSB, PIN 8 = MSB) to the D connector (4). PIN 24 is ground.

Logic Level	Volts	Current
0	0 to +0.8V	10 uA (max)
1	+2 to +5V	10 uA (max)

Fig. 4


On-Off
SYSTEM BLOCK DIAGRAM
Power Supply Module
Corcom
6J1
Voltage
Selecting-
Fused Connector
120/240V
50-60 Hz
Bridge
Rec-
tified
Gen.
Inst.
KBP-02
7824
+24
Signal
DP-241-7-24
35V
2200ufd


Out
AVR-E2-PG
2
PW
3
4
AMP
5
SL5
+24
1


PRF
AVR-CL
TRIG
INT
EXT
8
1
4
DELAY
9
2
6
3
7
SYNC
PRF RANGE

SYSTEM DESCRIPTION AND REPAIR PROCEDURE

The AVR-E2-C consists of the following basic modules:

1) AVR-E2-PG pulse generator module
2) AVR-E2-CL clock module
3) +24V power supply board

The modules are interconnected as shown in Fig. 4.

The clock module controls the output PRF and the relative delay between the main output and the SYNC outputs. The PG pulse generator modules generate the output pulse. In the event of an instrument malfunction, it is most likely that the rear panel 1.0A SB fuse or some of the output switching elements (SL5) may have failed due to an output short circuit condition or to a high duty cycle condition. The switching elements may be accessed by removing the cover plate on the bottom side of the instrument. NOTE: First turn off the prime power. The elements may be removed from their sockets by means of a needle nosed pliers. The SL5 is a selected VMOS power transistor in a TO 220 packages and may be checked on a curve tracer. If defective, replacement units should be ordered directly from Avtech. When replacing the SL5 switching elements, take care to insure that the short lead (of the three leads) is adjacent to the black dot on the chassis. If the switching elements are not defective, then the four Phillips screws on the back panel should be removed. The top cover may then be slid off and operation of the clock and power supply modules should be checked. The clock module is functioning properly if:

a) 0.1 usec TTL level outputs are observed at Pins 2 and 3.
b) The PRF of the outputs can be varied over the range of 50 Hz to 50 KHz using the PRF controls.
c) The relative delay between the Pin 2 and 3 outputs can be varied by at least 500 nsec by the DELAY controls.

The sealed clock module must be returned to Avtech for repair or replacement if the above conditions are not observed. The power supply board generates +24V DC to power the other modules. If the voltage is less than +24V, turn off the prime power and unsolder the lead from the 7824 regulator chip on the power supply board. Solder a 100 ohm 5 watt resistor to the 7824 output to ground and turn on the prime power. A voltage of +24 volts should be read. If the voltage is less then the power supply board is defective and should be repaired or replaced.

Schroff 06.11.91 Edition B

- EW
- EWD
- EA
- EAD
- OT
- OS