AVTECH ELECTROSYSTEMS LTD.

NANOSECOND WAVEFORM ELECTRONICS
ENGINEERING – MANUFACTURING

P.O. BOX 265
OGDENSBURG
NEW YORK
13669
(315) 472-5270

BOX 5120, STN. "F"
OTTAWA, ONTARIO
CANADA K2C 3H4
TEL: (613) 226-5772
FAX: (613) 226-2802

INSTRUCTIONS

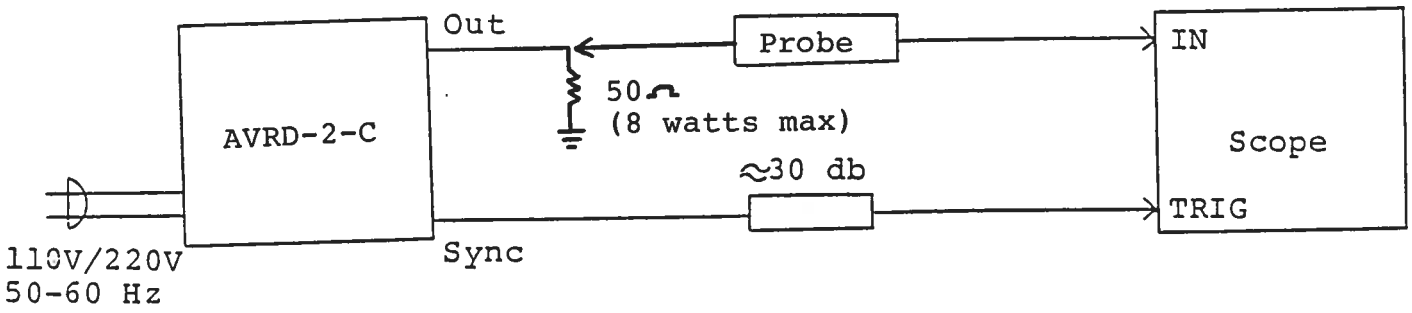
MODEL AVRD-2-C PULSE GENERATOR

S.N.:

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

Fig. 1 PULSE GENERATOR TEST ARRANGEMENT



Notes:

1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed 100 MHz.

2) The sync output channel provides TTL level signals. To avoid overdriving the TRIG input channel of some scopes, a 30 db attenuator should be placed at the input to the scope trigger channel.

3) To obtain a stable output display the PW, PRF and PRF FINE controls on the front panel should be set mid range. The front panel TRIG toggle switch should be in the INT position. The DELAY controls and the scope triggering controls are then adjusted to obtain a stable output. The scope may then be used to set the desired PRF by rotating the PRF and PRF FINE controls.

4) The output pulse widths for the positive and negative outputs are controlled by means of the front panel one turn PW P and PW N controls.

5) The output pulse amplitudes for the positive and negative outputs are controlled by means of the front panel one turn AMP P and AMP N controls.

6) The fall time from the positive going pulse to the negative going pulse is controlled by the TF one turn control and must be adjusted to minimize the fall time whenever the PW P setting is changed.

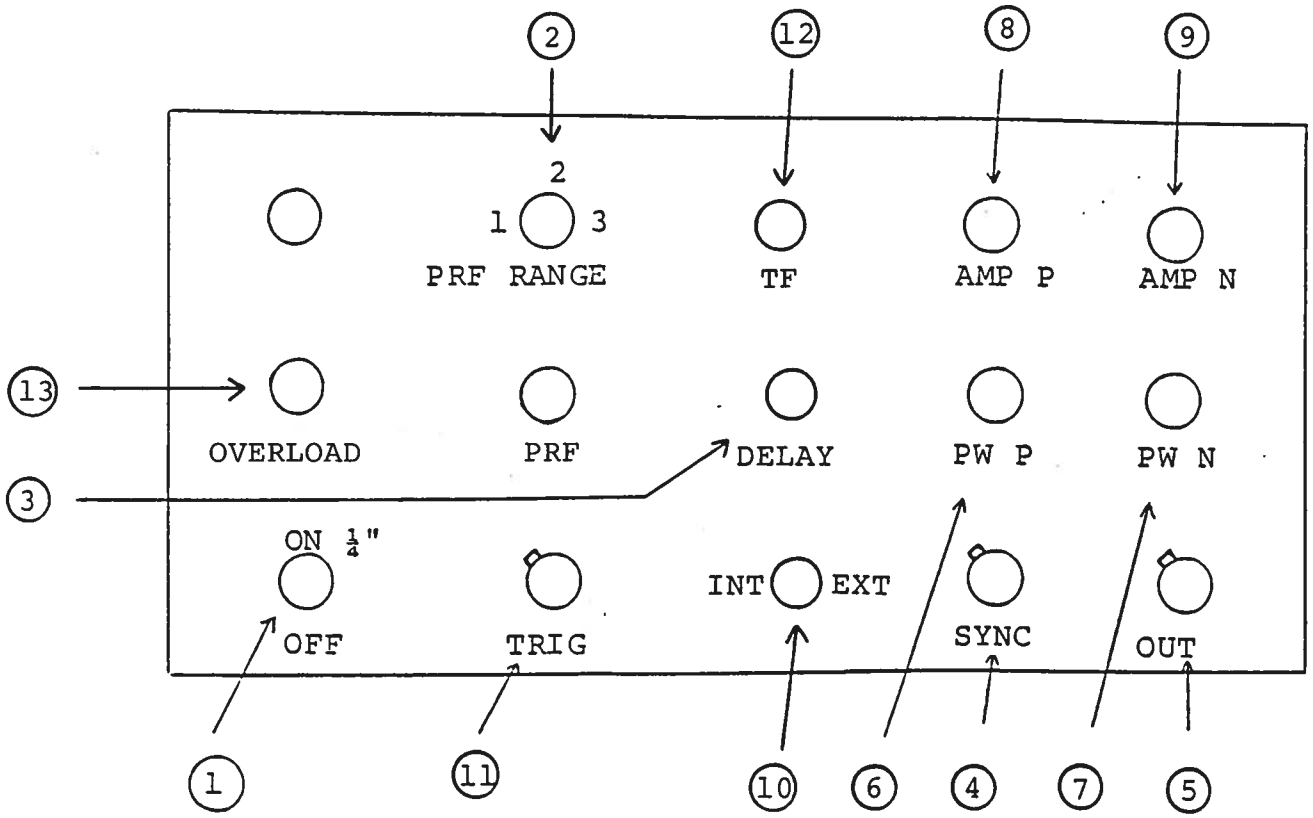
7) An external clock may be used to control the output PRF of the AVRD unit by setting the front panel TRIG toggle switch in the EXT position and applying a 0.2 usec (approx.) TTL level pulse to the TRIG BNC connector input. For operation in this mode, the scope time base must also be triggered by the external clock rather than from the SYNC output.

8) CAUTION: Care should be taken to not operate with an output pulse width greater than 1 usec as prolonged operation in this mode may very well result in equipment failure. Also, the maximum PRF or duty cycle must not be exceeded for the same reason. Under simultaneous conditions of wide pulse width, high PRF and high load current, the bias voltage applied to the output power stage decreases and as a result the attainable output peak voltage decreases to less than 100 volts. Under conditions of severe loading the output stage may be damaged.

9) AVRD units with a serial number higher than 5600 are protected by an automatic overload protective circuit which controls the front panel overload light. If the unit is overloaded (by operating at an exceedingly high duty cycle or by operating into a short circuit), the protective circuit will turn the output of the instrument OFF and turn the indicator light ON. The light will stay ON (i.e. output OFF) for about 5 seconds after which the instrument will attempt to turn ON (i.e. light OFF) for about 1 second. If the overload condition persists, the instrument will turn OFF again (i.e. light ON) for another 5 seconds. If the overload condition has been removed, the instrument will turn on and resume normal operation. Overload conditions may be removed by:

1) Reducing PRF (i.e. switch to a lower range)
2) Reducing pulse width (i.e. switch to a lower range)
3) Removing output load short circuit (if any)

Fig. 2 FRONT PANEL CONTROLS



(1) ON-OFF Switch. Applies basic prime power to all stages.

(2) PRF Controls. Varies PRF from 10 Hz to 20 KHz as follows:

Range 1	10	Hz		20 Hz
Range 2	10	Hz	to 2	KHz
Range 3	100	Hz	to 20	KHz

(3) DELAY Control Controls the relative delay between the reference output pulse provided at the SYNC output (4) the main output (5) and (6). This delay is variable over the range of 0 to about 1.0 usec.

(4) SYNC Output. This output precedes the main output (5) and is used to trigger the scope time base. The output is a TTL level 100 nsec (approx.) pulse capable of driving a fifty ohm load.

(5) OUT Connector. BNC connector provides output to a fifty ohm load.

(6) PW P Control. A one turn control which varies the positive output pulse width from 50 nsec to 1 usec.

(7) PW N Control. A one turn control which varies the negative output pulse width from 50 nsec to 1 usec.

(8) AMP P Control. A one turn control which varies the positive output pulse amplitude from 0 to +100V to a fifty ohm load.

(9) AMP N Control. A one turn control which varies the negative output pulse amplitude from 0 to -100V to a fifty ohm load.

(10) EXT-INT Control. With this toggle switch in the INT position, the PRF of the AVRD unit is controlled via an internal clock which in turn is controlled by the PRF and PRF FINE controls. With the toggle switch in the EXT position, the AVRD unit requires a 0.2 usec TTL level pulse applied at the TRIG input in order to trigger the output stages. In addition, in this mode, the scope time base must be triggered by the external trigger source.

(11) TRIG Input. The external trigger signal is applied at this input when the EXT-INT toggle switch is in the EXT position.

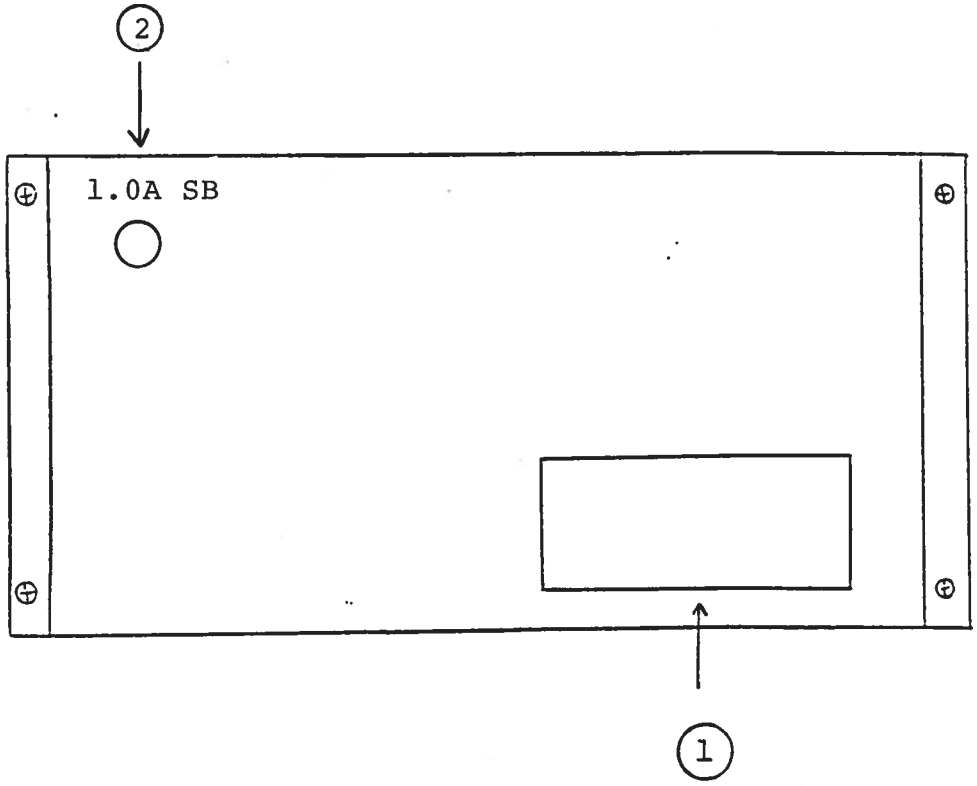
(12) TF. The transition time from the positive going pulse to the negative going pulse is controlled by the TF control. Setting must be adjusted to minimize the fall time whenever the PW P setting is changed.

(13) AVRD units with a serial number higher than 5600 are protected by an automatic overload protective circuit which controls the front panel overload light. If the unit is overloaded (by operating at an exceedingly high duty cycle or by operating into a short circuit), the protective circuit will turn the output of the instrument OFF and turn the indicator light ON. The light will stay ON (i.e. output OFF) for about 5 seconds after which the instrument will attempt to turn ON (i.e. light OFF) for about 1 second. If the overload condition persists, the instrument will turn OFF again (i.e. light ON) for another 5 seconds. If the overload condition has been removed, the instrument will turn on and resume normal operation. Overload conditions may be removed by:

1) Reducing PRF (i.e. switch to a lower range)
2) Reducing pulse width (i.e. switch to a lower range)
3) Removing output load short circuit (if any)

Fig. 3

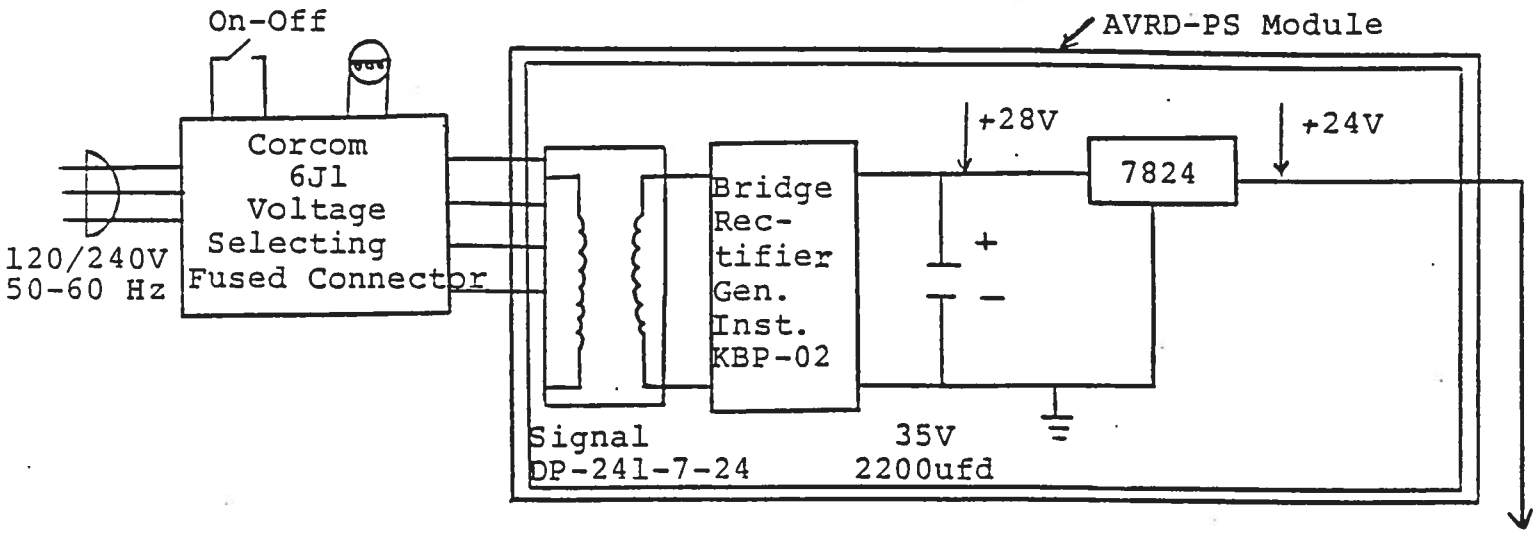
BACK PANEL CONTROLS



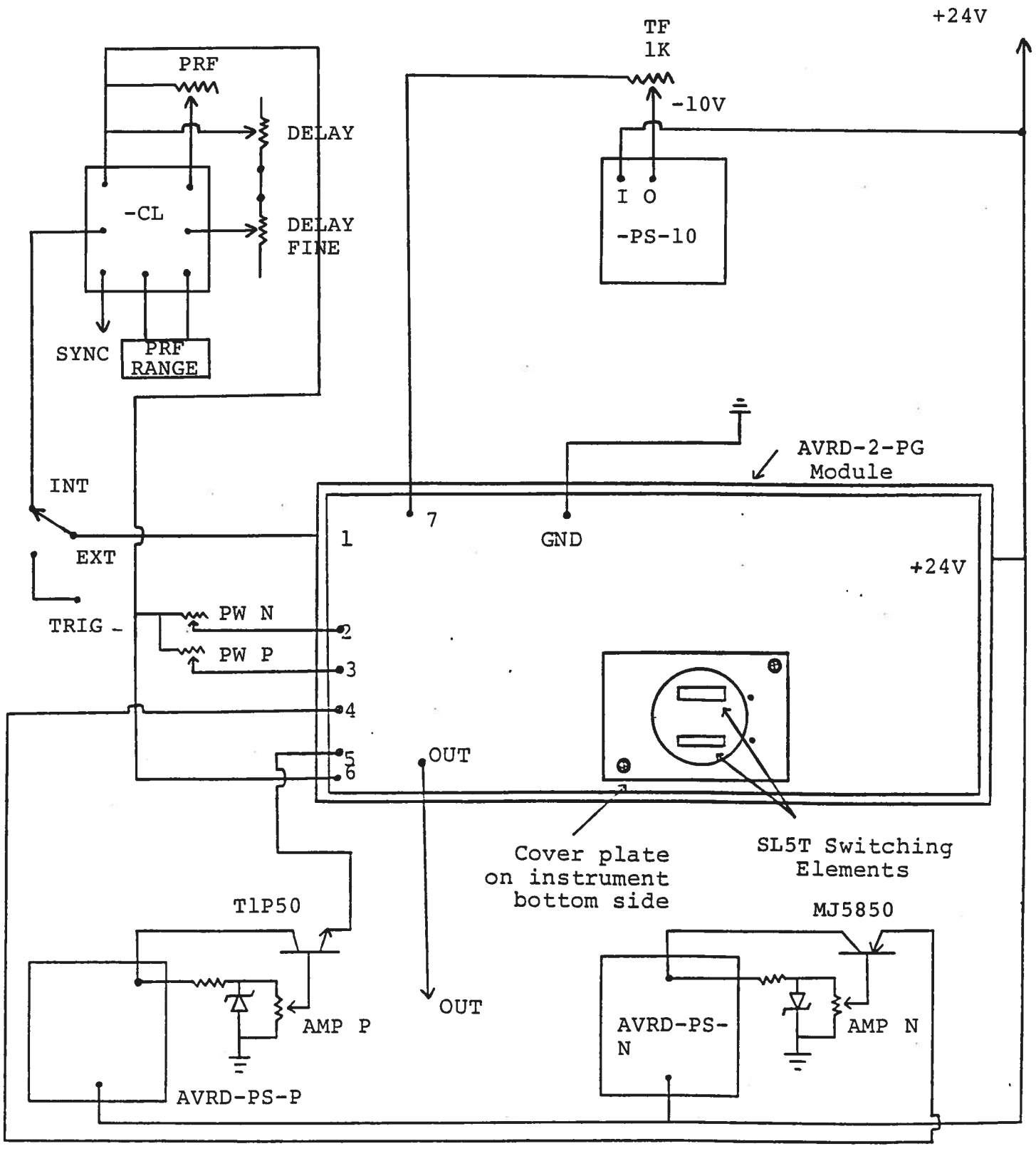
(1) FUSED CONNECTOR, VOLTAGE SELECTOR. The detachable power cord is connected at this point. In addition, the removable cord is adjusted to select the desired input operating voltage. The unit also contains the main power fuse.

(2) 1.0A SB. Fuse which protects the output stage if the output duty cycle rating is exceeded.

C. DC POWER SUPPLY



AVRD-2-C BLOCK DIAGRAM



SYSTEM DESCRIPTION AND REPAIR PROCEDURE

The AVRD-2-C consists of the following basic modules:

1) AVRD-2-PG pulse generator module
2) AVRD-CL clock module
3) +24V power supply board
4) AVRD-2-PS power supply modules (P and N)
5) AVRD-PS-10 module

The modules are interconnected as shown in Fig. 4. The clock module controls the output PRF and the relative delay between the main output and the SYNC outputs. The PG pulse generator modules generate the output pulse. In the event of an instrument malfunction, it is most likely that some of the output switching elements (SL5T) may have failed due to an output short circuit condition or to a high duty cycle condition. The switching elements may be accessed by removing the cover plate on the bottom side of the instrument. NOTE: First turn off the prime power. The elements may be removed from their sockets by means of a needle nosed pliers. The SL5T is a selected VMOS power transistor in a TO 220 packages and may be checked on a curve tracer. If defective, replacement units should be ordered directly from Avtech. When replacing the SL5T switching elements, take care to insure that the short lead (of the three leads) is adjacent to the black dot on the chassis. If the switching elements are not defective, then the four Phillips screws on the back panel should be removed. The top cover may then be slid off and operation of the clock and power supply modules should be checked. The clock module is functioning properly if:

a) 0.1 usec TTL level outputs are observed at pins 2 and 3.
b) The PRF of the outputs can be varied over the range of 1 Hz to 20 KHz using the PRF control.
c) The relative delay between the pin 2 and 3 outputs can be varied by at least 500 nsec by the DELAY controls.

The sealed clock module must be returned to Avtech for repair or replacement if the above conditions are not observed. The power supply board generates +24V DC to power the other modules. If the voltage is less than +24V, turn off the prime power and unsolder the lead from the 7824 regulator chip on the power supply board. Solder a 100 ohm 5 watt resistor to the 7824 output to ground and turn on the prime power. A voltage of +24 volts should be read. If the voltage is less then the power supply board is defective and should be repaired or replaced.

Schroff 08.19.91 Edition B

- PN