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## INSTRUCTIONS

MODEL AVR-65-C-FOICA PULSE GENERATOR

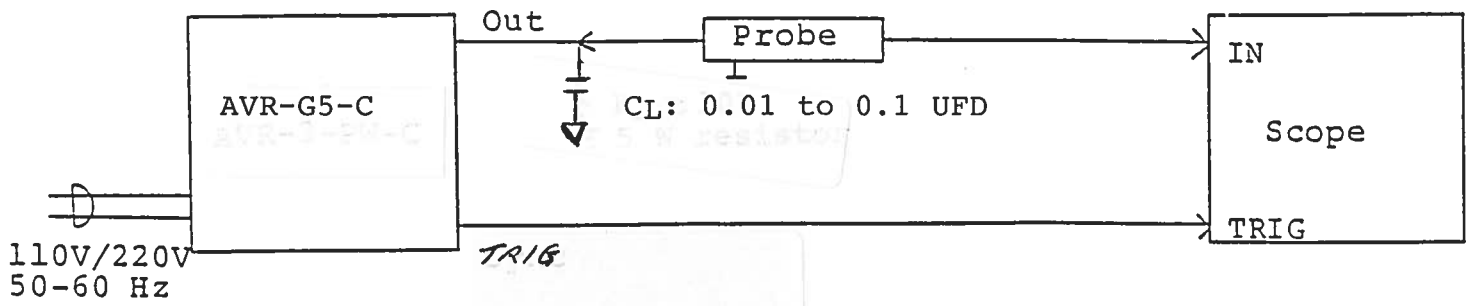
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## WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been disassembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

Fig. 1

PULSE GENERATOR TEST ARRANGEMENT



Notes:

- 1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed 50 MHz.
- 2) This unit was specifically designed to drive high impedance loads ( $R_L > 100K$ ,  $C_L$  0.01 to 0.1 ufd). The unit may fail if operated into low impedance loads (eg. 50 ohms).
- 3) The output pulse widths for the positive and negative swings are controlled by means of the front panel one turn PW controls and by the PW RANGE controls. The minimum and maximum PW for each range are as follows:

	<u>PW_P</u>	
Range 1	5 usec	10 usec
Range 2	10 usec	100 usec
Range 3	100 usec	10 msec
Range 4	1.0 msec	10 msec
Range 5	10 msec	100 msec

	<u>PW_N</u>	
Range 1	10 usec	100 msec
Range 2	100 usec	1 msec
Range 3	1 msec	10 msec
Range 4	10 msec	100 msec
Range 5	100 msec	1 sec

To voltage control the output pulse width within each range, set the rear panel switch in EXT position and apply 0 to +10 volts between terminal A and ground ( $R_{IN} > 10K$ ). (option).

- 4) Note that the output pulse repetition frequency is effectively controlled by the settings of the PW P and the PW N controls.

- 5) CAUTION: Extreme caution must be exercised when operating with PW of less than about 100 usec. The duty cycle must be maintained as low as possible, preferably less than 20% (eg. for PW P of 100 usec, the PW N should be greater than about 400 usec. This is particularly important for high  $C_L$  (eg. 0.1 ufd). If the duty cycle is too high, the rear panel 1.0 A SB fuse will blow and in extreme cases the output switching elements (SL22T) may fail. The fuse rating was deliberately set low (1.0A) so as to protect the output switching elements from abuse relating to high duty cycle operation.
- 6) The output pulse amplitudes for the positive and negative swings are controlled by means of the front panel one turn AMP control. To voltage control the output amplitude, set the rear panel switch in the EXT position and apply 0 to +10 volts between terminal A and ground ( $R_{IN} > 10K$ ). (option).
- 7) The TRIG output channel provides TTL level signals. The TRIG output lags the main output.

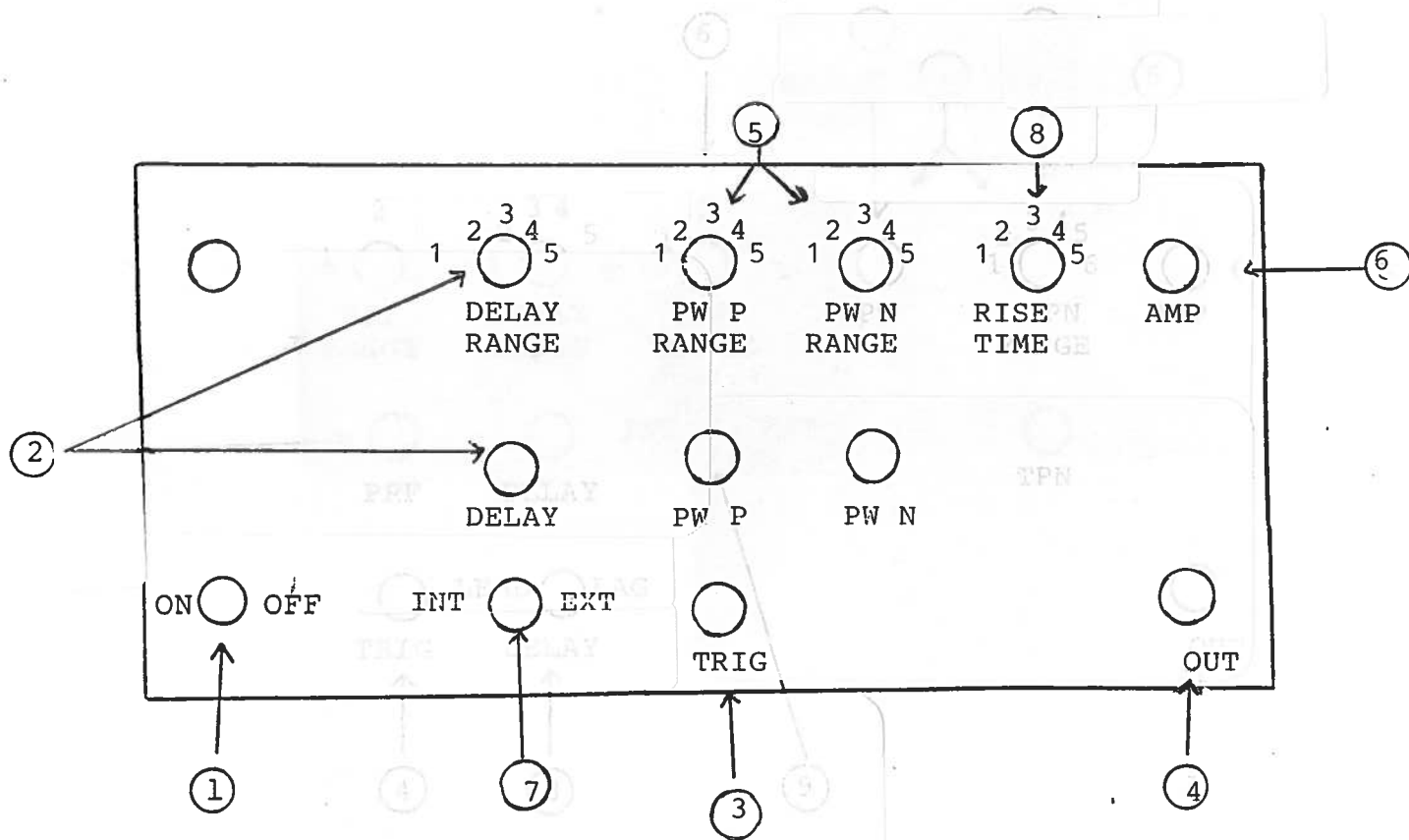
The DELAY control controls the relative delay between the reference output pulse provided at the TRIG output and the main output. This delay is variable over the range of 1.0 usec to 100 msec, as follows:

	MIN	MAX
Range 1	1 usec	10 usec
Range 2	10 usec	100 usec
Range 3	100 usec	1.0 msec
Range 4	1.0 msec	10 msec
Range 5	10 msec	100 msec

- 8) The output rise, fall time is controlled by the five position rise time switch and the load capacitance. The switch inserts a series resistance (5, 10, 50, 200 and 500 ohm) in the load path and the resulting rise time is determined by this resistance and load capacitance ( $T_R \approx 3 R C_L$ ).
- 9) An external clock may be used to control the output PRF (and PW P, PW N) of the AVR unit by setting the front panel TRIG toggle switch in the EXT position and applying a TTL level pulse to the TRIG BNC connector input. The output PW P is then equal to the TTL high level interval while the PW N is equal to the TTL low level interval. For operation in this mode, the scope time base must also be triggered by the external clock rather than from the TRIG output.

Fig. 2

FRONT PANEL CONTROLS



- (1) ON-OFF Switch. Applies basic prime power to all stages.
- (2) DELAY Control. Controls the relative delay between the reference output pulse provided at the TRIG output (3) the main output (4). This delay is variable over the range of 1.0 usec to about 100 msec as follows:

	MIN	MAX
Range 1	1 usec	10 usec
Range 2	10 usec	100 usec
Range 3	100 usec	1 msec
Range 4	1 msec	10 msec
Range 5	10 msec	100 msec

- (3) TRIG Output. This output is used to trigger the scope time base. The output is a TTL level 100 nsec (approx.) pulse capable of driving a fifty ohm load. This output lags the output at (4). The external trigger signal is applied at this input when the EXT-INT toggle switch is in the EXT position.
- (4) OUT Connector. BNC connector provides output to a high impedance load ( $C_L$  0.01 to 1.0 ufd,  $R_L > 100K$ ).
- (5) PW P, PW N: The output pulse widths for the positive and negative swings are controlled by means of the front panel one turn PW controls and by the PW RANGE controls. The minimum and maximum PW for each range are as follows:

	<u>PW P</u>	
Range 1	5 usec	10 usec
Range 2	10 usec	100 usec
Range 3	100 usec	10 msec
Range 4	1.0 msec	10 msec
Range 5	10 msec	100 msec

	<u>PW N</u>	
Range 1	10 usec	100 msec
Range 2	100 usec	1 msec
Range 3	1 msec	10 msec
Range 4	10 msec	100 msec
Range 5	100 msec	1 sec

To voltage control the output pulse width within each range, set the rear panel switch in EXT position and apply 0 to + 10 volts between terminal A and ground ( $R_i > 10K$ ). (option).

Note that the output pulse repetition frequency is effectively controlled by the settings of the PW P and the PW N controls.

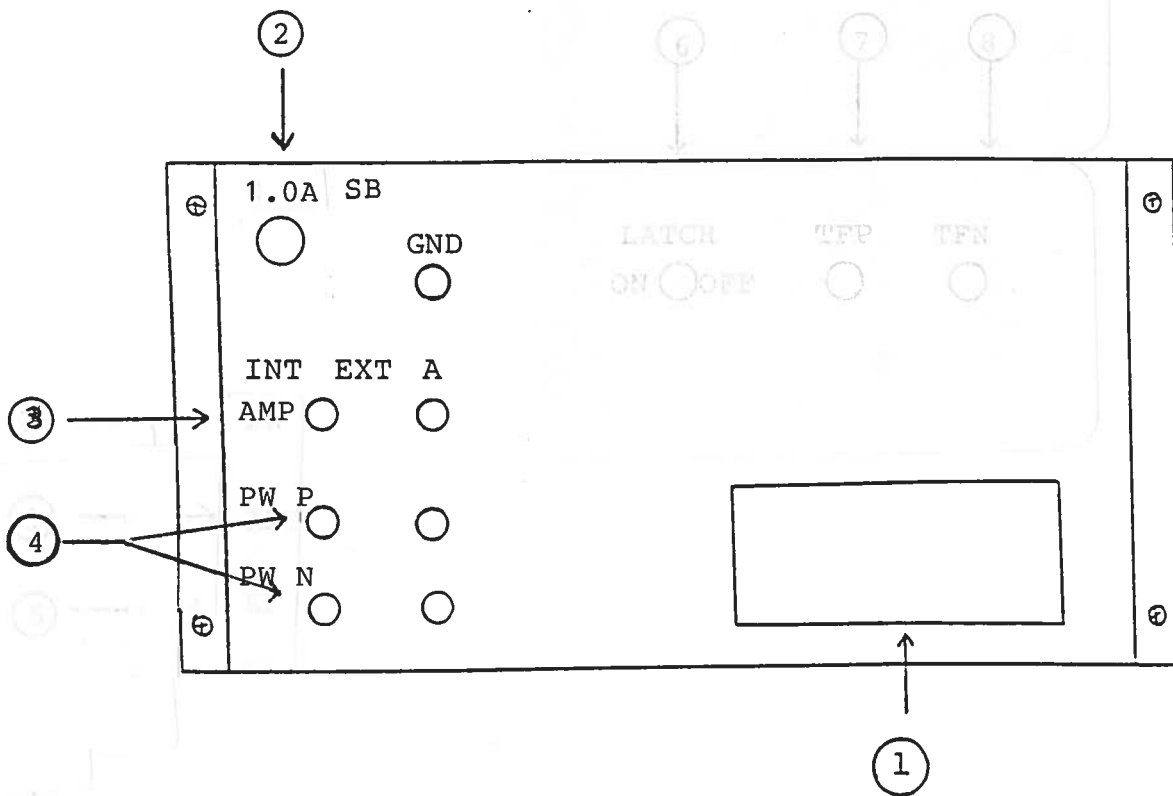
CAUTION: Extreme caution must be exercised when operating with PW of less than about 100 usec. The duty cycle must be maintained as low as possible, preferably less than 20% (eg. for PW P of 100 usec, the PW N should be greater than about 400 usec. This is particularly important for high  $C_L$  (eg. 0.1 ufd). If the duty cycle is too high, the rear panel 1.0 A SB fuse will blow and in extreme cases the output switching elements (SL22T) may fail. The fuse rating was deliberately set low (1.0A) so as to protect the output switching elements from abuse relating to high duty cycle operation.

- (6) AMP Control. A one turn control which varies the output pulse amplitude from 0 to  $\pm 220$  V to a high impedance load.
- (7) EXT-INT Control. With this toggle switch in the INT position, the PRF of the AVR unit is controlled via an internal clock which in turn is controlled by the PW P and PW N controls. With the toggle switch in the EXT position, the AVR unit requires a TTL level pulse applied at the TRIG input in order to trigger the output stages. The output PW P is then equal to the TTL high level interval while the PW N is equal to the TTL low level interval. For operation in this mode, the scope time base must also be triggered by the external clock rather than from the TRIG output.
- (8) RISE TIME Control. The output rise, fall time is controlled by the five position rise time switch and the load capacitance. The switch inserts a series resistance (5, 10, 50, 200 and 500 ohm) in the load path and the resulting rise time is determined by this resistance and load capacitance ( $T_R \approx 3 R_C C_L$ ).



Fig. 3

BACK PANEL CONTROLS



- (1) FUSED CONNECTOR, VOLTAGE SELECTOR. The detachable power cord is connected at this point. In addition, the removable card is adjusted to select the desired input operating voltage. The unit also contains the main power fuse (0.5A 5B).
- (2) 1.0A 5B. Fuse which protects the output stage if the output duty cycle rating is exceeded.
- (3) EA. To voltage control the output amplitude, set the switch in the EXT position and apply 0 to +10 volts between terminal A and ground ( $R_{IN} > 10K$ ). (option).
- (4) EW. To voltage control the output pulse width, (within each range) switch in the EXT position and apply 0 to +10 volts between terminal A and ground ( $R_{IN} > 10K$ ). (option).

## SYSTEM DESCRIPTION AND REPAIR PROCEDURE

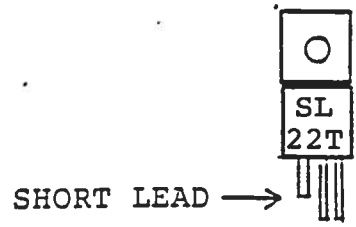
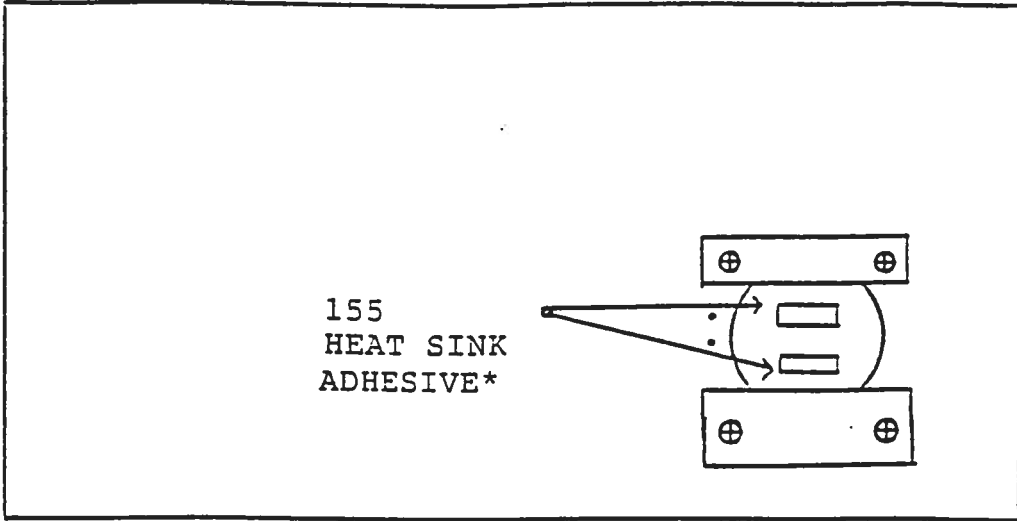
The AVR-65-C-FOICA consists of the following basic modules:

- 1) AVR-65-FOICA-PG pulse generator module
- 2) AVR-65-FOICA-PW pulse switch module
- 3) +24V power supply board
- 4) AVR-65-FOICA-PS power supply module
- 5) AVR-65-FOICA-EW pulse switch modules (P and N)
- 6) AVR-65-FOICA-DL delay module

In the event of an instrument malfunction, it is most likely that the rear panel 1.0A SB fuse or some of the output switching elements (SL22T) may have failed due to an output short circuit condition or to a high duty cycle condition. The switching elements may be accessed by removing the cover plate on the bottom side of the instrument. **NOTE:** First turn off the prime power. **CAUTION:** Briefly ground the SL22T tabs to discharge the 250 volts power supply potential. The elements may be removed from their sockets by means of a needle nosed pliers after removing the four counter sunk 2-56 Phillips screws which attach the small aluminum heat sinks to the body of the instrument. The SL22T is a selected VMOS power transistor in a TO 220 package and may be checked on a curve tracer. If defective, replacement units should be ordered directly from Avtech. When replacing the SL22T switching elements, take care to insure that the short lead (of the three leads) is adjacent to the back of the chassis. (See following Fig.). The SL22T elements are electrically isolated from the small copper heat sink but are bonded to the heat sinks using WAKEFIELD TYPE 155 HEAT SINK ADHESIVE. If the switching elements are not defective, then the four Phillips screws on the back panel should be removed. The top cover may then be slid off and operation of the power supply modules checked. The sealed clock module must be returned to Avtech for repair or replacement if the above conditions are not observed. The power supply board generates +24V DC to power the other modules. If the voltage is less than +24V, turn off the prime power and unsolder the lead from the 7824 regulator chip on the power supply board. Solder a 100 ohm 5 watt resistor to the 7824 output to ground and turn on the prime power. A voltage of +24 volts should be read. If the voltage is less then the power supply board is defective and should be repaired or replaced.

SL22T HEAT SINKING

BACK



POWER SUPPLY

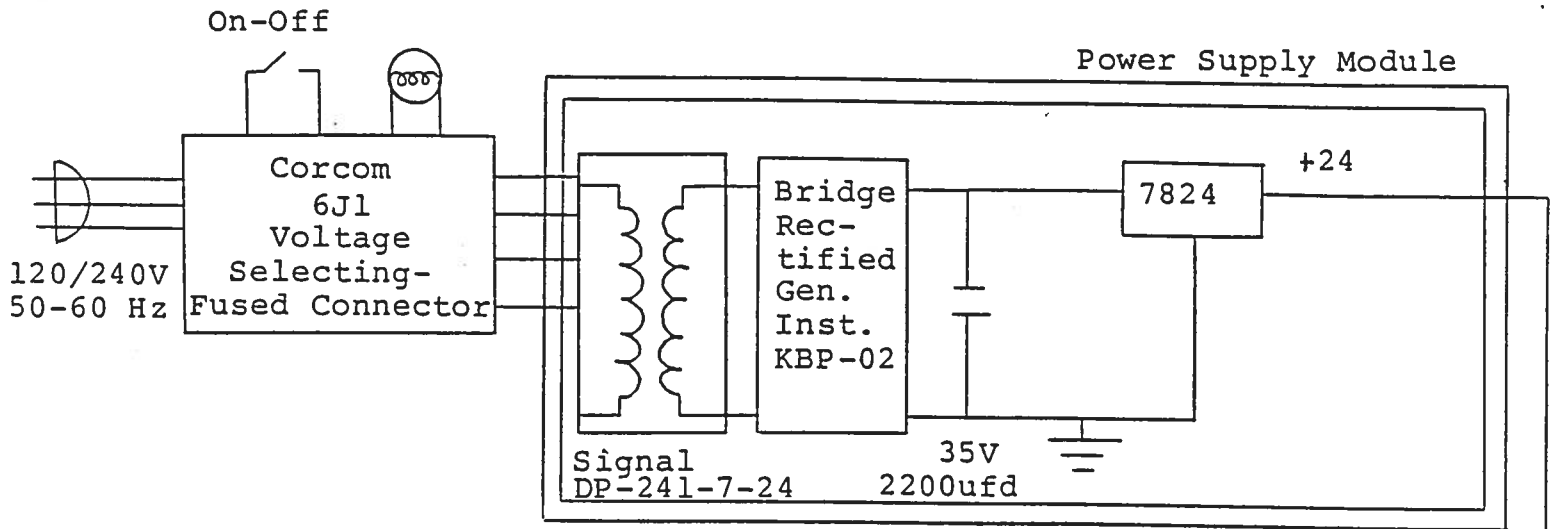


Fig. 3b

### RECOMMENDED PRELIMINARY TEST PROCEDURE

- 1) Connect to load and scope as shown in Fig. 1. Use a low  $C_L$  load (eg. 0.01 ufd). Prime power should be OFF.
- 2) Rotate AMP fully counter clockwise.
- 3) Set PW P in range 2 (MID range).
- 4) Set PW N in range 3 (MID range).
- 5) Set Rise time in position 1.
- 6) Set delay in Range 1 (MID range).
- 7) Set INT-EXT in INT.
- 8) Set scope vertical on 50 volts/DIV and time base on 1 ms/DIV. Set time base to trigger on positive edge of trigger signal from pulse generator.
- 9) Turn on prime power and adjust time scope base controls to insure that scope is triggering.
- 10) Set AMP control mid range and obtain waveform as shown in Photo A.
- 11) Adjust time base setting to 5 us/DIV to obtain display shown in Photo B. It may be necessary to fine tune the delay setting on the pulse generator and on the scope time base.
- 12) Set the rise time control on position 5 to obtain display shown in photo C.
- 13) Adjust AMP and PW P and PW N as required but do not exceed duty cycle of 20% for PW of less than 100 us.  
  
Note that if the rear panel 1.0A SB fuse blows repeatedly then the duty cycle must be reduced, particularly if the  $C_L$  is very high. (Reduce duty cycle by increasing the PW N setting).
- 14) Photo D illustrates a high duty cycle output ( $\approx$  50 %) (5.0 ms/DIV) which may safely be generated at wide pulses (eg. 10 ms).
- 15) Note that the output rise time is directly proportional to the load capacitance. Consequently it is necessary to re-adjust the rise time control when the load capacitance is changed (in order to maintain a specific rise time).

Schroff

12.27.90

-EW

-EA

1. The first part of the report is devoted to a description of the system and its components. It is assumed that the reader is familiar with the basic concepts of the system and its components.

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