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INSTRUCTIONS

Model AVR-W-C-S1 Pulse Generator

S.N.:

WARRANTY

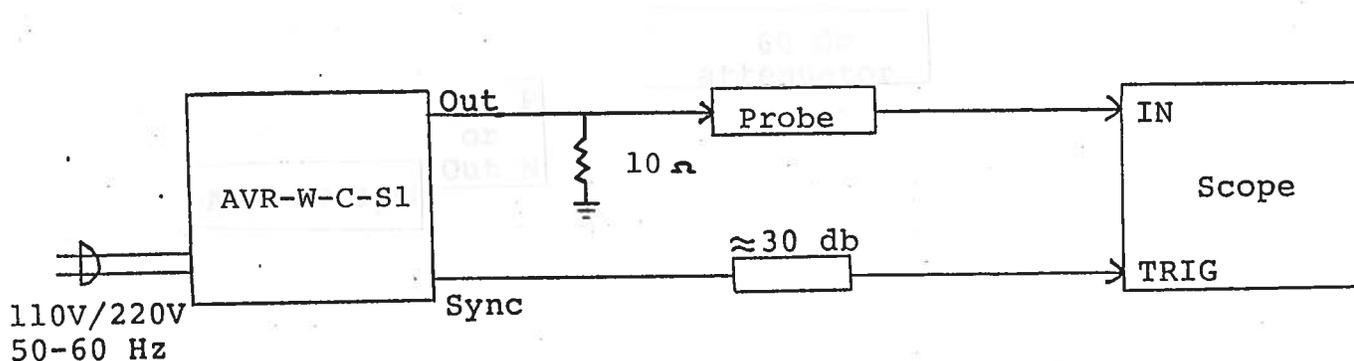
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Fig. 1

PULSE GENERATOR TEST ARRANGEMENT



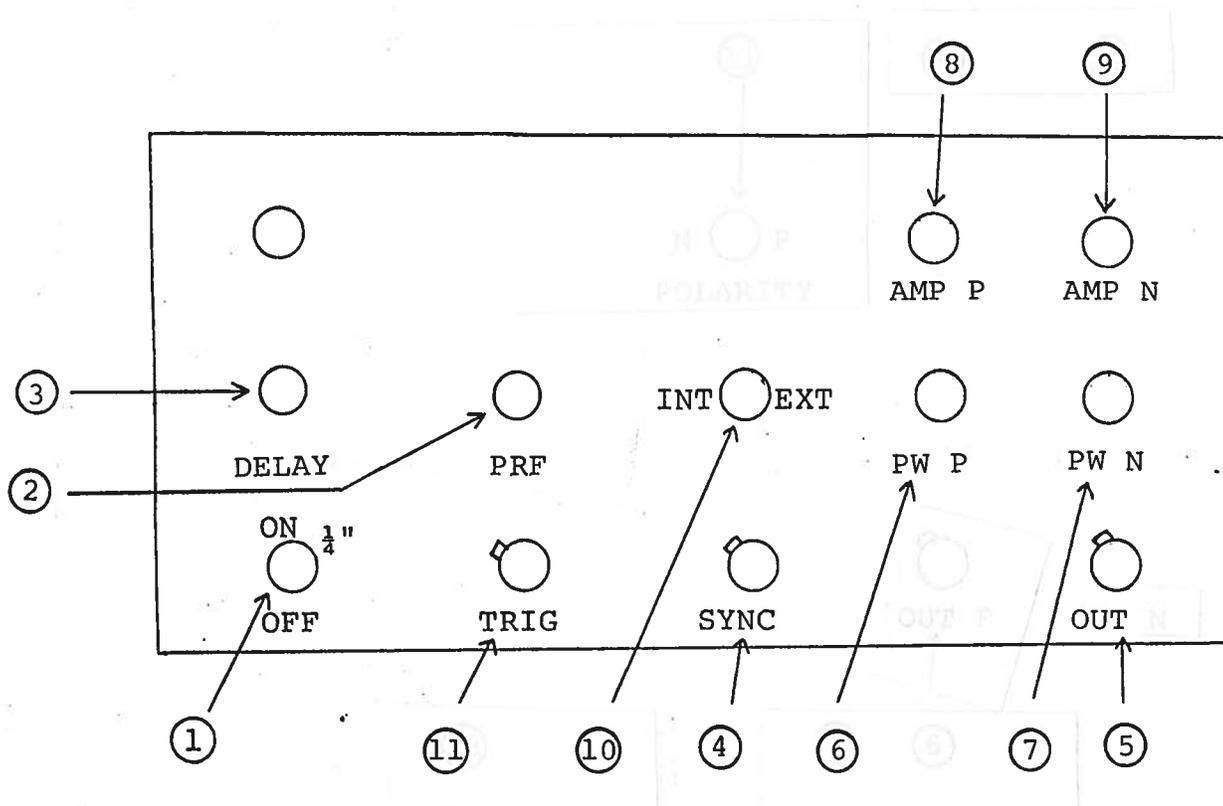
Notes:

- 1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed 50 MHz.
- 2) The sync output channel provides TTL level signals. To avoid overdriving the TRIG input channel of some scopes, a 30 db attenuator should be placed at the input to the scope trigger channel.

- 3) To obtain a stable output display the PW and PRF controls on the front panel should be set mid-range. The front panel TRIG toggle switch should be in the INT position. The DELAY controls and the scope triggering controls are then adjusted to obtain a stable output. The scope may then be used to set the desired PRF by rotating the PRF control.
- 4) The output pulse widths for the positive and negative swings are controlled by means of the front panel one turn PW P and PW N controls.
- 5) The output pulse amplitudes for the positive and negative swings are controlled by means of the front panel one turn AMP P and AMP N controls.
- 6) An external clock may be used to control the output PRF of the AVR unit by setting the front panel TRIG toggle switch in the EXT position and applying a 0.2 usec (approx.) TTL level pulse to the TRIG BNC connector input. For operation in this mode, the scope time base must also be triggered by the external clock rather than from the SYNC output.

Fig. 2

FRONT PANEL CONTROLS

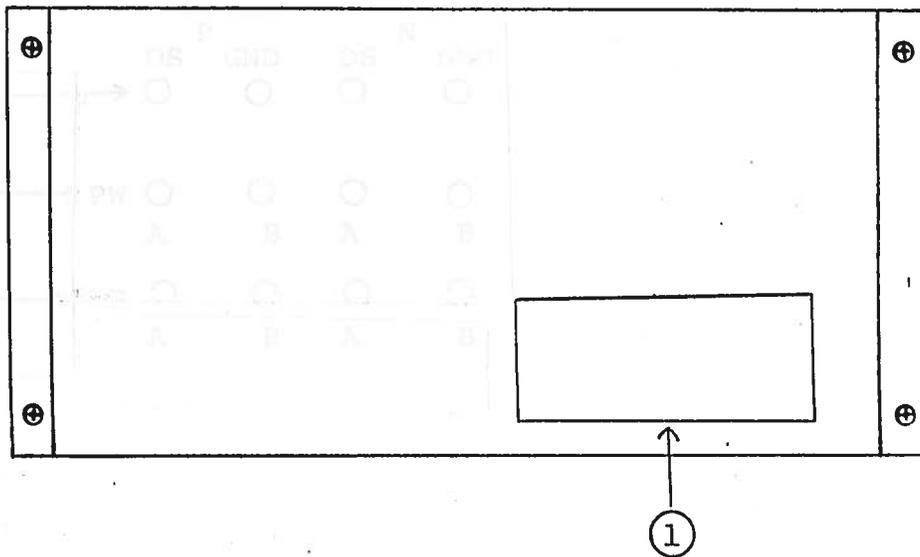


- ① ON-OFF Switch. Applies basic prime power to all stages.
- ② PRF Control. Varies PRF from 50 Hz to 1 KHz.
- ③ DELAY Control. Controls the relative delay between the reference output pulse provided at the SYNC output ④ and the main output ⑤. This delay is variable over the range of 0 to about 200 usec.
- ④ SYNC Output. This output either precedes (by up to 0.5 usec) or follows (by up to 200 usec) the main output ⑤ and is used to trigger the scope time base. The output is a TTL level 100 nsec (approx.) pulse capable of driving a fifty ohm load.
- ⑤ OUT Connector. BNC connector provides output to a 10 ohm load.
- ⑥ PW P Control. A one turn control which varies the positive output pulse width from 25 to 100 usec.
- ⑦ PW N Control. A one turn control which varies the negative output pulse width from 25 to 100 usec.

- ⑧ AMP P Control. A one turn control which varies the positive output pulse amplitude from 0 to +10V to a 10 ohm load.
- ⑨ AMP N Control. A one turn control which varies the negative output pulse amplitude from 0 to -20V to a 10 ohm load.
- ⑩ EXT-INT Control. With this toggle switch in the INT position, the PRF of the AVR unit is controlled via an internal clock which in turn is controlled by the PRF and PRF FINE controls. With the toggle switch in the EXT position, the AVR unit requires a 0.2 usec TTL level pulse applied at the TRIG input in order to trigger the output stages. In addition, in this mode, the scope time base must be triggered by the external trigger source.
- ⑪ TRIG Input. The external trigger signal is applied at this input when the EXT-INT toggle switch is in the EXT position.

Fig. 3

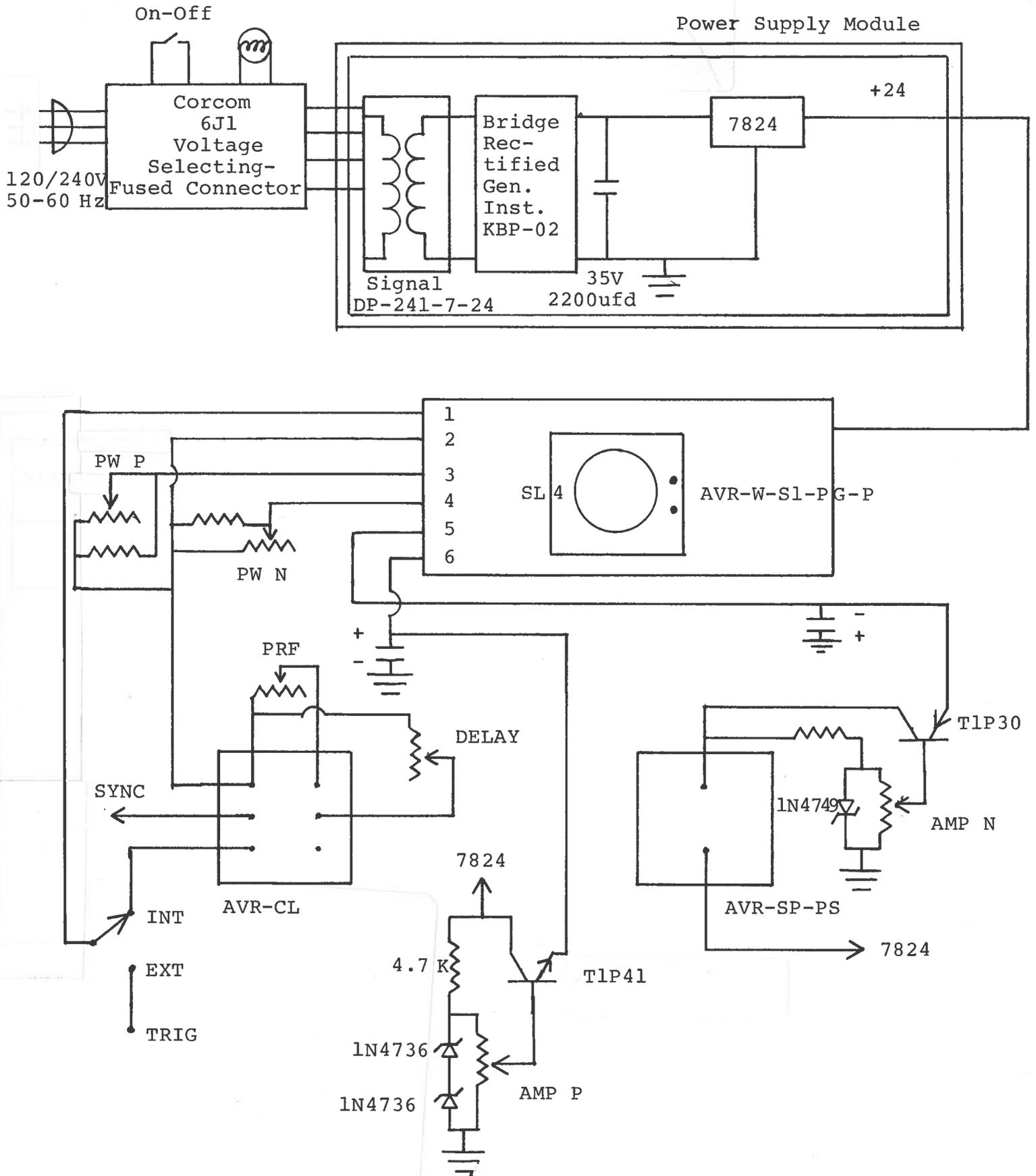
BACK PANEL CONTROLS



- ① FUSED CONNECTOR, VOLTAGE SELECTOR. The detachable power cord is connected at this point. In addition, the removable cord is adjusted to select the desired input operating voltage. The unit also contains the main power fuse.

Fig. 4

SYSTEM BLOCK DIAGRAM



SYSTEM DESCRIPTION AND REPAIR PROCEDURE

The AVR-W-C-S1 consists of the following basic modules:

- 1) AVR-W-S1-PG pulse generator modules
- 2) AVR-1-CL clock module
- 3) AVR-SP-PS power supply module
- 4) +24V power supply board

The modules are interconnected as shown in Fig. 4. The clock module controls the output PRF and the relative delay between the main output and the SYNC outputs. The PG pulse generator modules generate the output pulse.

In the event of an instrument malfunction, it is most likely that some of the output switching elements (SL4) may have failed due to an output short circuit condition or to a high duty cycle condition. The switching elements may be accessed by removing the cover plate on the bottom side of the instrument. NOTE: First turn off the prime power. The elements may be removed from their sockets by means of a needle nosed pliers. The SL4 is a selected VMOS power transistor in a TO 220 packages and may be checked on a curve tracer. If defective, replacement units should be ordered directly from Avtech. When replacing the SL4 switching elements, take care to insure that the short lead (of the three leads) is adjacent to the black dot on the chassis.

If the switching elements are not defective, then the four Phillips screws on the back panel should be removed. The top cover may then be slid off and operation of the clock and power supply modules should be checked. The clock module is functioning properly if:

- a) 0.1 usec TTL level outputs are observed at pins 2 and 3.
- b) The PRF of the outputs can be varied over the range of 50 Hz to 1 KHz using the PRF control.
- c) The relative delay between the pin 2 and 3 outputs can be varied by at least 200 usec by the DELAY controls.

The sealed clock module must be returned to Avtech for repair or replacement if the above conditions are not observed.

The power supply board generates +24VDC to power the other modules. If the voltage is less than +24V, turn off the prime power and unsolder the lead from the 7824 regulator chip on the power supply board. Solder a 100 ohm 5 watt resistor to the 7824 output to ground and turn on the prime power. A voltage of +24 volts should be read. If the voltage is less then the power supply board is defective and should be repaired or replaced.

Schroff

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