# AVTECH ELECTROSYSTEMS LTD.

NANOSECOND WAVEFORM ELECTRONICS
ENGINEERING – MANUFACTURING

P.O. BOX 265
OGDENSBURG
NEW YORK
13669
(315) 472-5270

BOX 5120, STN. "F"
OTTAWA, ONTARIO
CANADA K2C 3H4
TEL: (613) 226-5772
FAX: (613) 226-2802
TELEX: 053-4591


## INSTRUCTIONS

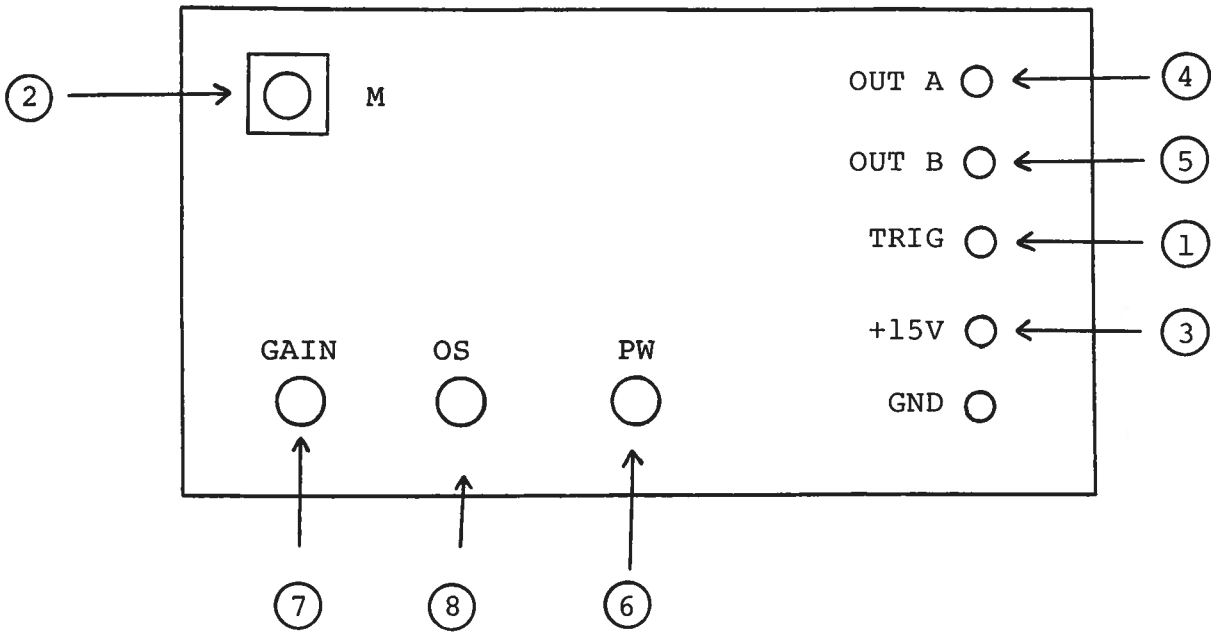
## MODEL AVS-100B-GSSA SAMPLE AND HOLD UNIT

S.N.:

## WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

## FRONT PANEL CONTROLS



(1) TRIGGER. Solder terminal to which TTL level 50 nsec to 1.0 usec trigger pulse is applied to activate sampler. Sample is taken 35.5 nsec after the leading edge of the input TRIGGER pulse.

(2) M (MONITOR) Output. SMA connector provides a +1 volt replica of the sample pulse to a fifty ohm load. The width of the M output pulse is controlled by the 10 turn PW control and is equal to the width of the sample pulse which operates the sampling gate (0.1 to 1.0 nsec). The M output appears 37.5 nsec after the application of the TRIGGER pulse. The input signal is sampled 2 nsec before the leading edge of the M output.

(3) +15V. Apply DC prime power to this solder terminal (I approx. 550 mA).

(4) OUT A. Solder terminal connects 3 usec wide pulse output to fifty ohm load. Output amplitude equals IN amplitude (GAIN control adjusts this). DC offset when IN amplitude equals zero set to zero using OS control.

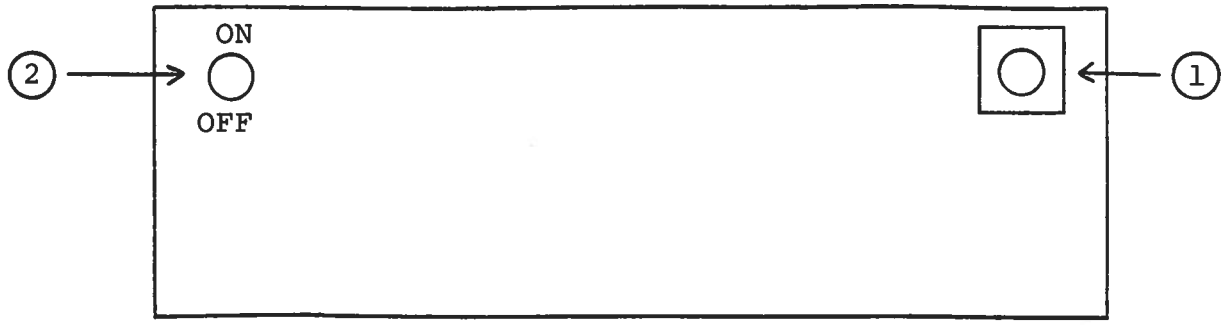
(5) OUT B. Solder terminal connects DC output to fifty ohm load. Output amplitude equals IN amplitude (GAIN control adjusts this). DC offset when IN amplitude equals zero set to zero using OS control.

(6) PW Control. A ten turn control which varies the M (and sample) pulse width from 0.1 to 1.0 nsec (shipped with PW set at about 0.1 nsec). Note that pulse width is measured at 80% of maximum amplitude (since gate operation occurs at the peak of the pulse).

(7) GAIN Control. A one turn control used to set OUT amplitude equal to IN amplitude.

(8) OS Control. A ten turn offset control used to set OUT amplitude equal to zero when IN amplitude equals zero.

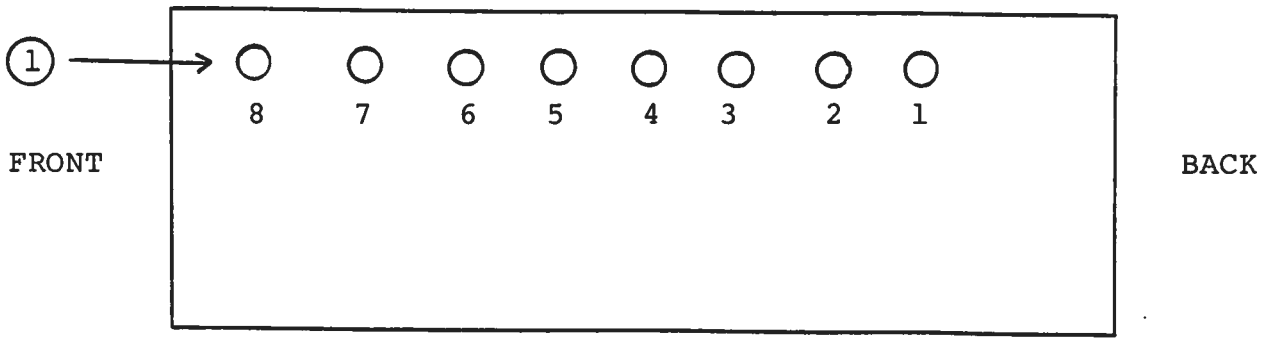
## BACK PANEL CONTROLS



(1) IN. SMA connector, fifty ohm input impedance to which signal to be sampled is applied. Max input ±1 volt.

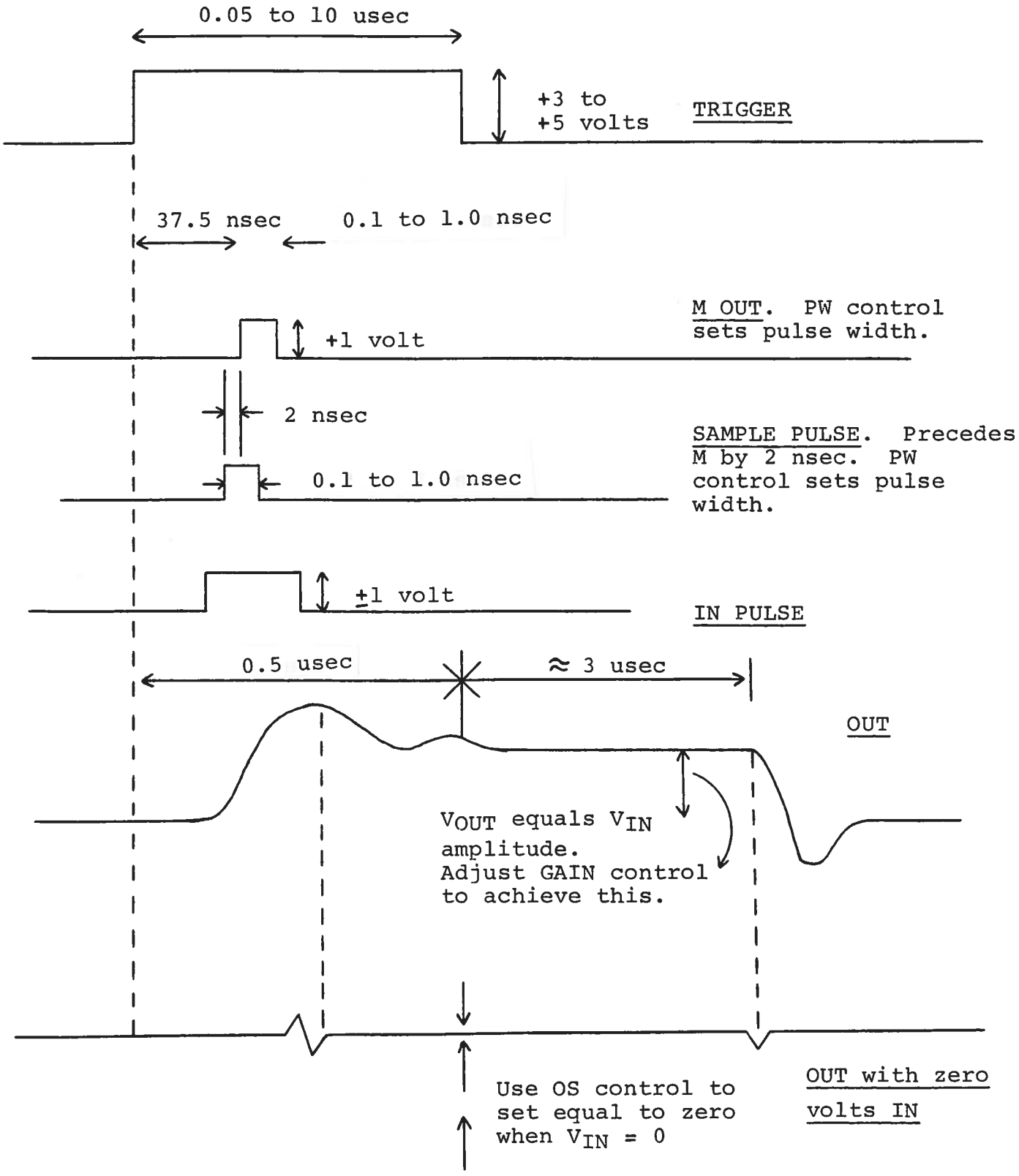
(2) ON-OFF. Two position switch controls discharge gate action. Note that if discharge gate function is turned off, output amplitude typically rises by a factor of about 3 (for a gate width of 100 ps) and so the gain must then be reduced by a factor of about 3.

## SIDE PANEL CONTROLS




(1) BASE LINE ADJUSTMENT POTS. See paragraphs 8 and 9 of Test Procedures.

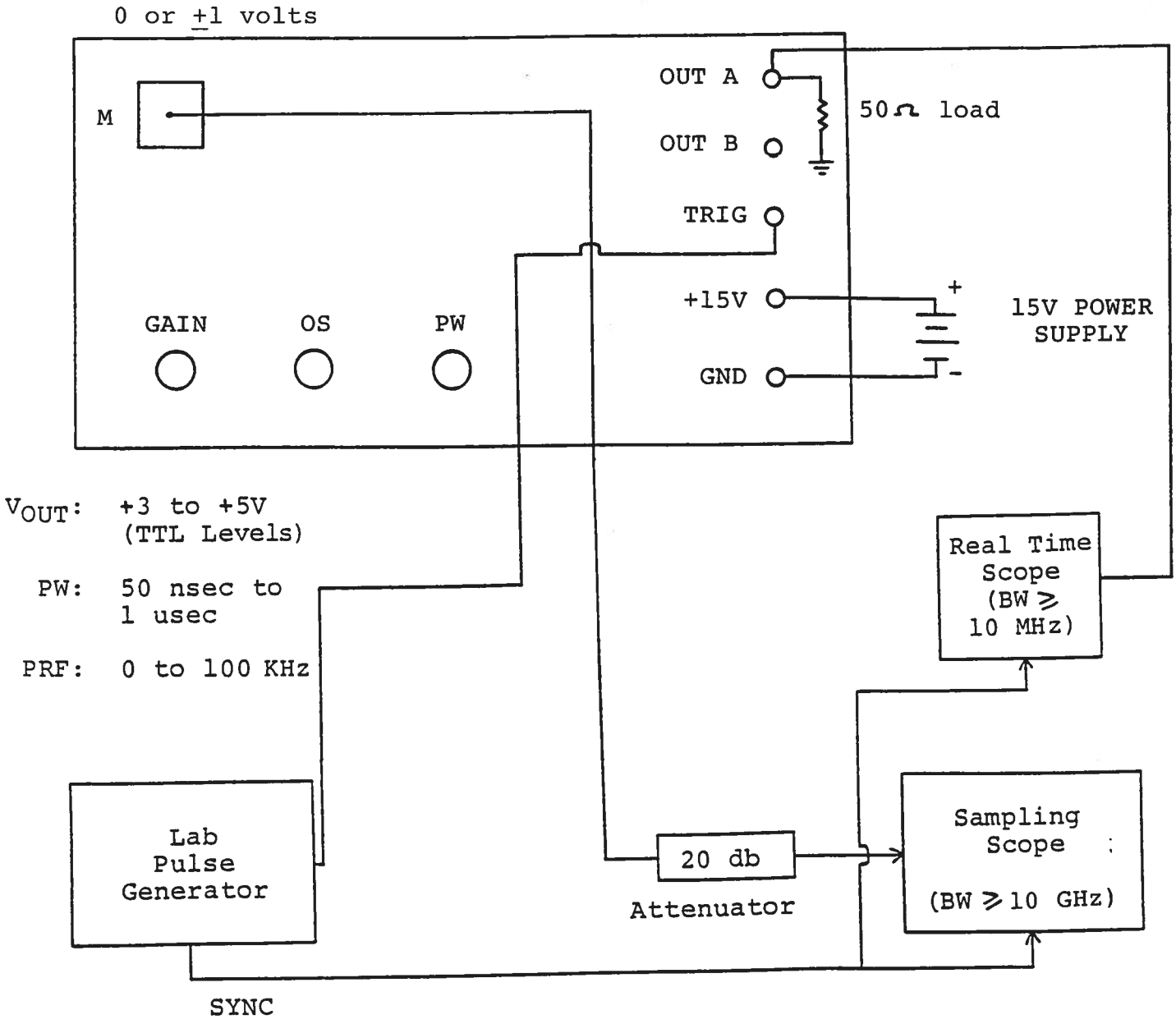
# TIMING WAVEFORMS



# TEST PROCEDURE AND OPERATION INSTRUCTIONS

1) It is recommended that the AVS-100 unit be first tested and calibrated using a DC input signal rather than a short pulse input signal so as to avoid the requirement of syncronizing the sampling pulse and the input pulse.

2) The following arrangement may be used for the DC test:


0 or ±1 volts
M
OUT A
OUT B
TRIG
+15V
GND
50Ω load
+
-
15V POWER SUPPLY
GAIN
OS
PW
$V_{OUT}$: +3 to +5V (TTL Levels)
PW: 50 nsec to 1 usec
PRF: 0 to 100 KHz
Real Time Scope (BW ≥ 10 MHz)
Lab Pulse Generator
20 db
Attenuator
Sampling Scope
(BW ≥ 10 GHz)
SYNC

3) Apply prime power and with sampling scope and back panel PW control, set sampling pulse (or M) to desired width (see timing waveforms). Unit shipped with PW set at about 1 nsec. Allow several minutes for warm-up.

4) Apply 0 volts to IN input and use real time scope and OS control to set OUT level to approximately zero volts. (see timing waveforms).

5) Apply + or -1 volts to IN input and adjust GAIN control to obtain + or -1 volt at OUT point (see timing waveforms) and at the DC OUT point.

6) The unit is now calibrated. Note that if PW of sample pulse is changed, it will be necessary to reset the GAIN control. Increasing the PW increases the output amplitude thereby requiring that the GAIN control be turned counter clockwise to again set the OUT amplitude equal to the IN amplitude.

7) The unit may now be tested with a short pulse applied to the IN port. It should not be necessary to readjust the OS or GAIN controls. Note that if the amplitude of the input pulse is known (eg. determined using the sampling scope) the unit may be calibrated using only the short pulse rather than using the DC levels.

8) When operating properly, the pulse output should appear as a train of approx. 4 usec pulses having the same polarity and amplitude as the nanosecond pulses applied at the IN port. The base line between the pulses should be near zero and constant (or horizontal). If the base line between the pulses is not constant it may not be possible to calibrate the unit as previously described or the output amplitude may be a function of the PRF. It is recommended that the PRF be set at 500 Hz to adjust the base line. Normally only pots 7 and 8 should be adjusted to attain a constant base line level between the pulses. Note that only very minor adjustments of the pots should be necessary. Once the base line is horizontal, it may be zeroed using the OS control.

9) As the PW sample width is varied from 0.1 to 1.0 nsec, the OUT level during the 3 usec pulse out interval may vary and it may not be possible to zero using the rear panel OS control. In such cases, a minor change in the PW control may make a zero output possible. If this is not possible then minor adjustment to pots 1 and 2 on the module can be made to establish a zero output.

# SYSTEM DESCRIPTION

See pages 70 and 71 of Cat. No. 7.

The sampler attenuates the signal applied at the IN port and takes a 0.1 to 1.0 nsec wide sample of this signal. The resulting sample voltage is stored on a small capacitor which shunts the high impedance input buffer amplifier. The capacitor is discharged to zero after 3.5 usec by a shunting switch. Variable gain output amplifiers boost the capacitor voltage so that the output voltage equals the amplitude of the voltage applied to the IN terminal of the AVS-100 unit.

12.05.90

-M